DEC-11-HRKA-D

RK11-C
moving head
disk drive controller
manual

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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CONTENTS

CONTENTS (cont)

ILLUSTRATIONS

TABLES

INTRODUCTION

The purpose of this manual is to provide the user with the theory of operation and logic descriptions necessary to understand and maintain the RK11-C Moving Head Disk Drive Controller System. The level of discussion assumes that the reader is familiar with basic PDP-11 operation. The manual contains both general and detailed descriptions of the RK11-C Moving Head Disk Drive Controller unit, hereafter designated RK11 or RK11 Control. Coverage of the disk drives is found in the respective manuals supplied with the disk drive used in the particular disk drive control system. A general description of the disk drive and its options is presented in Chapter 1.

Although control signals and data are transferred between the RK11 Control and the Unibus, it is beyond the scope of this manual to cover operation of the bus itself. A detailed description of the Unibus is presented in the *PDP-11 Unibus Interface Manual* (DEC-11-HIAA-D).

A copy of this manual is included with each RK11 Disk Drive Control System that is purchased. In various places within this manual engineering drawings are referenced. These engineering drawings are found in Volume 2 entitled RK11 Disk Drive Control Engineering Drawings. This volume reflects the updated RK11 drawings at the time the equipment is shipped and is to be used in conjunction with this manual.

This manual is divided into six major chapters: Introduction, General Description, Programming, Detailed Description, Installation, and Maintenance.

CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The RK11 Disk Drive Controller System is a PDP-11 Computer peripheral (see Figure 1-1) that is interfaced to the computer by the Unibus. The RK11 System serves as an additional random-access memory unit to the PDP-11 System. Each RK11 Disk Drive Controller System consists of a RK11 Control and from one to eight optional disk drive units. The disk drive unit options are the RK02, RK03, RK04, or RK05. The RK11 Control interfaces the particular disk drive configuration to the Unibus. Also, the RK11 converts serial data off the disk drive to parallel data on the Unibus and vice versa. Therefore, the RK11 Disk Drive Controller System reads and writes serial memory information in parallel transfer to, or from, the PDP-11 Unibus. The RK11 is completely supported by the PDP-11 Disk-Operating Software System.

1.2 FUNCTIONAL DESCRIPTION

The RK11 Control and the Disk Drive combine as a complete mass-storage system for the PDP-11. The system stores digital data in serial format on IBM 2315 type disk cartridges. The data can be randomly accessed in blocks or sectors through movable read/write heads and, when necessary, protected from overwriting. The system provides the option for either low- or high-density disk drives in which one disk drive with one RK11 provides storage for either 600K words or 1.2 million words, respectively. The number of disk drives is expandable up to eight drives per RK11 Control, which provides 4.8 million words (low density) or 9.6 million words (high density). The high- and low-density disk drives can be mixed for one RK11 in any configuration up to eight drives. Additional RK11 Control units can be installed on a PDP-11. The disk drives are interfaced with the RK11 Control by a cable that carries both control and data information between them (see Figure 1-2).

1.2.1 Disk Drive Units

The RK11 disk drive unit consists of the movable head drive logic and the removable disk cartridge. The disk drive is available as either high- or low-density disk drive options. The high-density option provides a choice of either the RK03 Diablo Disk Drive Unit or the RK05 DECpack Unit, both utilizing the RK03-KA, IBM Type 2315 12-sector high-density disk cartridge. The low-density option provides a choice of either the RK02 Diablo Disk Drive Unit or the RK04 DECpack Unit, both utilizing the RK02-KA IBM Type 2315 12-sector low-density disk cartridge.

The removable disk cartridge offers virtually unlimited off-line capacity, with rapid transfer of files between on-line and off-line without duplicating operations. Each disk cartridge is permanently mounted inside a protective case that automatically opens when inserted into the disk drive. When the cartridge is on-line, a highly-efficient continuous air-filtration system prevents dust contamination. The IBM Type 2315 disk cartridge consists of 12 sectors of 128 words (low density) or 256 words (high density). Each cartridge contains 203 cylinders of two tracks per cylinder.

The disk drive consists of the logic circuitry that enables data to be written on or read from a disk cartridge. Also, the disk drive contains the logic that positions the movable read/write heads. The disk drive uses voice coil head positioning for the RK04 and RK05 disk drives and rack and pinion head positioning for the RK02 and RK03 disk drives. These contribute to high reliability and an average total access time of 90 ms. Detailed descriptions and discussions of the disk drive logic are found in the manual supplied with the disk drive used in a particular RK11 Disk Drive Control System.

1.2.2 RK11 Control Unit

The RK11 Control Unit (RK11-C) is a rotating, mass-memory control capable of communicating with high- or low-density drives in any combination up to a maximum configuration of eight drives per control. The RK11 Control serves as the interface between the disk drives and the PDP-11 Unibus. The RK11 is data block oriented, but is capable of transferring from 1 to 2^{16} consecutive words without reinitiation or processor intervention. The RK11 connects directly to the Unibus and communicates with the processor for status and control information. For data information, the RK11 communicates directly with the memory without processor supervision. This level of communication, called non-processor request (NPR), is the PDP-11 feature that allows the RK11 to transfer data directly to, or from, the memory. All RK11 data transfers use NPR communication.

The RK11 contains eight 16-bit hardware registers for communication with the processor and memory. These registers are listed in Table 1-1, with their respective abbreviation and address designations. These device registers initiate all RK11 System software control and can be read or written into using software instructions that refer to their respective addresses. A detailed description of the registers and their bit assignments is presented in Chapter 3.

The RK11 Control performs five major logic operations: control, non-data transfer, data transfer, error detection, and maintenance. The RK11 uses these logical operation areas to perform any one of eight data or non-data transfer functions. The data transfer functions are the Write, Write Check, and Read functions; the non-data transfer functions are the Control Reset, Seek, Read Check, Drive Reset, and Write Lock functions. A data transfer function is one in which data is transferred from a disk drive, through the RK11 Control, and out onto the Unibus. A Read Check operation transfers data from the disk drive to the RK11 Control but not onto the Unibus; therefore, it is a non-data transfer function. See Figure 1-3 for the RK11 block diagram.

Through the control logic, the software operating system initializes the RK11 by selecting the disk drive to be used, the cylinder address on the disk, the disk surface, and the sector within the cylinder (RKDA). Also, the number of words to be transferred (RKWC) and the location to which the transfer is to be made (RKBA) are loaded through the software operating system. One of the eight possible RK11 data or non-data transfer functions is then selected (function register bits of the RKCS).

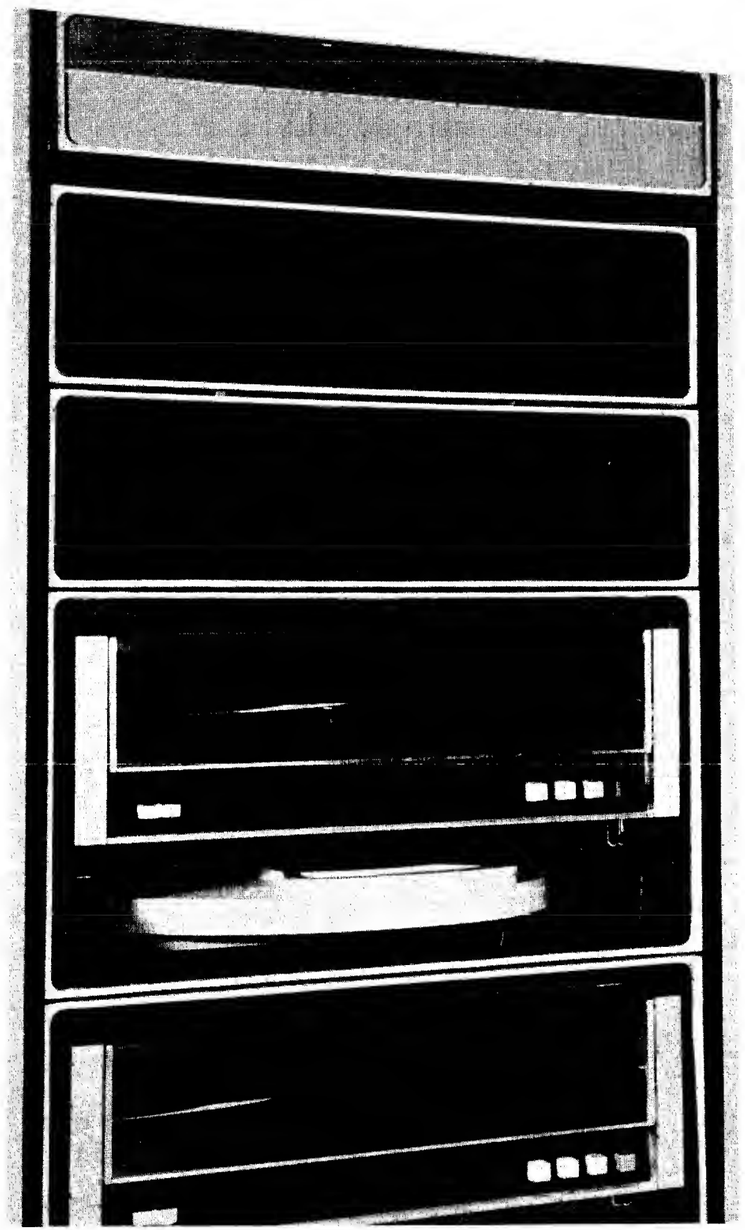


Figure 1-1 RK11 Disk Drive Control System

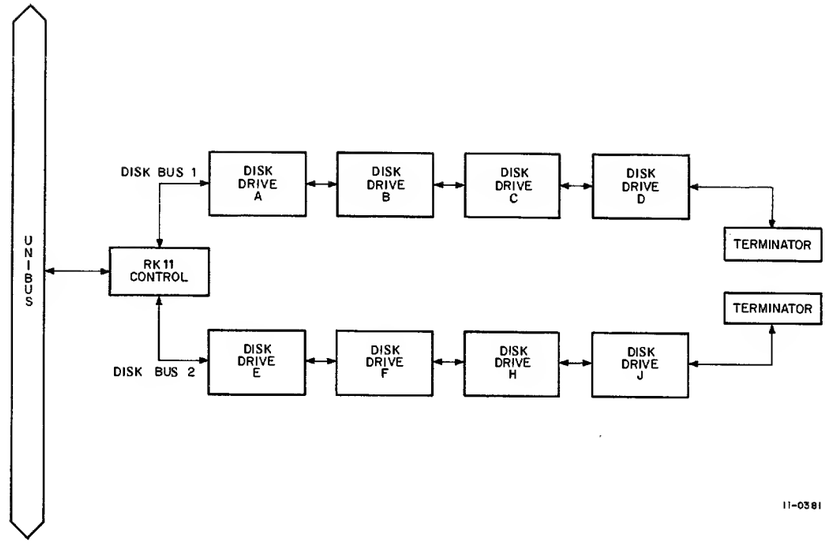


Figure 1-2 RK11 Disk Drive Control Block Diagram

Table 1-1
RK11 Hardware Registers

Register	Abbreviation	Address
Drive Status Register	RKDS	777400
Error Register	RKER	777402
Control Status Register	RKCS	777404
Word Count Register	RKWC	777406
Current Bus Address Register	RKBA	777410
Disk Address Register	RKDA	777412
Maintenance Register	RKMR	777414
Data Buffer Register	RKDB	777416

For all non-data transfer functions, except Read Check, the RK11 operation is limited. The Control Reset function clears all of the RK11 Control logic and is then ready for the next function. The Drive Reset function directs the disk drive to move its heads to the first or zero cylinder location of the disk cartridge. The Write Lock function puts the selected disk drive in Write Protect status. This function prevents any Write operation from occurring on that disk drive until the drive is manually reset to write enable. The Seek function directs a selected disk drive to move its heads to the cylinder location specified in the RKDA. When the drive has accepted the address and initiated the Seek function, the RK11 Control is free to perform another function, although the drive may not complete the Seek for some time. On expanded systems (more than one disk drive), Seek functions can be overlapped for efficiency; that is, one drive may perform one function while one or more additional drives are

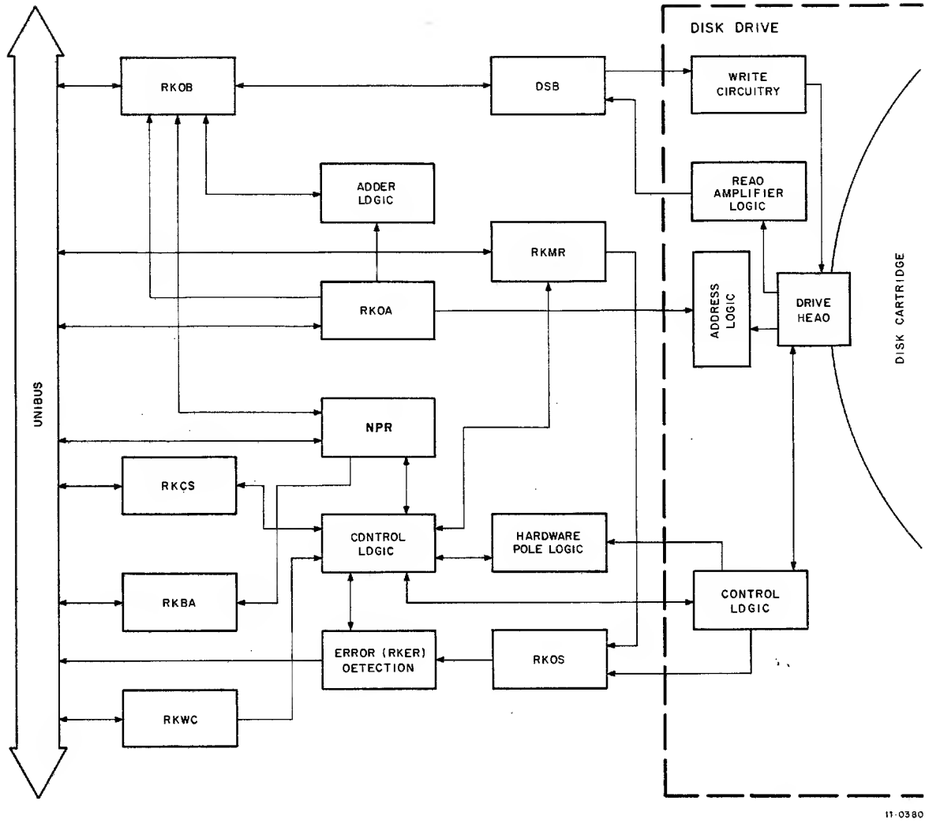


Figure 1-3 RK11 Block Diagram

seeking new head positions for the next function. Since one drive may take longer than another to complete the initiated Seek because of initial head location, a hardware poll logic operation is performed to determine when each drive finishes its Seek function. This operation informs the RK11 logic which drives are at the cylinder locations specified by their Seek functions. The RK11 can now perform other operations on any of the now available drives.

A Write, Write Check, or Read can be performed for data transfer functions. For each of these functions the RK11 performs an implied Seek to position the selected drive's heads at the correct cylinder location. However, if a Seek has already been performed to this cylinder location, the data transfer function will be initiated almost immediately with no head motion. At this point, the overlapped Seek functions previously discussed become significant in that the disk drives to perform data transfer can be located at specified cylinder locations before the transfer function is initiated. Once the implied Seek is performed, the RK11 Control reads the first header word encountered on the cylinder into the Data Serial Buffer (DSB). This header word is then loaded into the RKDB, and the RK11 then checks the header by comparing it with the cylinder address located in the RKDA. This comparison is done in the Adder logic of the RK11. If the comparison is favorable the Read, Write, or Write Check function continues. An unfavorable comparison causes an error condition in the Error Detection logic.

For a Read function, each data word of a sector on the disk is shifted into the DSB and then loaded into the RKDB. In the RKDB each data word generates an NPR that loads the data word onto the bus for transmission to the memory. For the Write function, the header is first loaded into the RKDB from the RKDA; then it is loaded into the DSB and serially shifted to the disk drive. Therefore, for a Write function the header is read, checked, and then re-written on the disk. As the header is being re-written, the NPR loads the first data word into the RKDB from the bus; from the bus it is loaded into the DSB and shifted out to the disk drive. This continues for each data word, since an NPR is generated for each word to be loaded into the RKDB for writing. A Write Check function first loads the word off the bus into the RKDB; the word is then loaded into the DSB. The corresponding word on the disk is shifted into the DSB. At this point, the DSB is shifting the disk drive word in one end of the DSB and shifting the bus word out of the other. At each end of the DSB Write Check compares each bit which should correspond since the data being Write Checked is the corresponding disk and memory data from a previous Write function. Any bit by bit discrepancy of the data being compared causes an error condition in the RK11 logic. These portions of each data transfer function are initiated when the correct sector is reached in the cylinder; this is indicated when the disk sector counter (RKDS) equals the sector address specified in the RKDA.

All data transfer functions are terminated when the RKWC indicates that the number of words designated to be transferred has been accomplished. This inhibits further NPR communication. However, if the RK11 has not yet reached the end of the sector it will continue to sequence through to the end of the sector although no data is transferred between the RK11 and the Unibus. At the end of the sector the RK11 will terminate all logic operation. During the data transfer function the Adder logic adds each word transferred per sector and shifts the 16-bit sum of all the sector words (checksum) to the RKDB after the last data word of the sector. For Read or Write Check this value is compared with the checksum value coming off the disk for any discrepancy. For a Write function, the calculated checksum value is loaded into the RKDB and then written onto the disk following the last data word of the sector being written. At the end of the sector the function will either continue, by again re-writing the header of the next sequential sector, or terminate, if the word count (RKWC) signaled function termination by overflowing. A change in cylinder for a data transfer function causes another implied Seek whereupon the header is checked and the function continues without interruption. However, a data transfer function cannot continue to another disk drive. An attempt to continue a function operation beyond one disk drive causes an Overrun error.

For all data transfer functions the control of the header, data, checksum, and sector boundary areas in the logic is governed by the disk format. This format is monitored in the RK11 Control by the Major State Logic (MSR) which is discussed in detail in Chapter 3. The disk format is discussed in Chapter 2. The MSR monitors the disk format through the RK11 bit counter and word count logic (discussed in Chapter 3), which count each bit and each word in each disk format area.

The only function not yet discussed is the Read Check function which, by definition, is a non-data transfer function. However, this function operates similarly to a data transfer function. The function starts as a Read function, with the implied Seek and the shifting of the header into the DSB from the disk for the header check. When the data is shifted into the DSB from the drive, it is loaded into the RKDB, but does not go out onto the bus since all NPRs are inhibited. All that occurs for each word is the operation of the Adder logic calculating the checksum. Therefore, the Read Check function is essentially a parity check of the disk data before performing a Read function. This parity check is realized when the checksum is read off the disk drive and compared with the checksum calculated by the Adder logic. Any discrepancy results in an error condition.

The RK11 Error Detection logic discussed in detail in Chapter 3, consists primarily of the conditions necessary to qualify the conditions of the RKER (Chapter 2) and the initiation of processor interrupts due to an error condition.

Finally, the system maintenance function simulates disk drive signals in the RK11 Control and is used exclusively for testing the RK11 System without any disk drives on the system. Detailed discussion of the maintenance function is found in Chapter 6.

1.3 SPECIFICATIONS

The RK11 System specifications are grouped into five general areas: physical description, environmental limits, logic format, timing format, and power requirements.

1.3.1 Physical Description

RK11 System housing is provided by a cabinet designed to house one RK11 Control and from one to four disk drives. An expanded system, with a maximum of eight disk drives, houses the remaining four drives in a second cabinet. Each cabinet contains individual power supplies for the units housed within. The RK11 Control is mounted at the top of the initial cabinet and uses its own H720 Power Supply that is located in the bottom front portion of the cabinet. The four possible disk drives are mounted one over the other with one H734 powering two of the drives (drives A and B) and another H734 powering the other two drives (C and D). **Other equipment should not be mounted in the RK11 System cabinets.**

Cabinet Dimensions:	Height:	71-7/16 in.
	Width:	21-11/16 in.
	Depth:	30 in.

1.3.2 Environmental Limits

This paragraph lists the environmental limits required for proper operation of the RK11 System.

Temperature:	(Operating) 60° to 110°F (with interchangability between reading and writing of the same data guaranteed for a 30°F temperature variation).
Relative Humidity:	(Operating) 20% to 80%
Condensation:	(Operating or Storage) None
Vibration/Shock:	(Operating) To prevent data errors, extreme vibrations should be avoided while the disk drive is transferring information.

1.3.3 Logic Format

This paragraph lists the logic format pertaining to data transfer and data storage in the RK11 System.

Drive Format: (All Drives)	1 Disk/Drive 203 Cylinders/Drive 2 Surfaces/Drive 2 Tracks/Cylinder 12 Sectors/Track	
Word Format:	Low Density (RK02, RK04)	High Density (RK03, RK05)
Data Words/Sector	$128_{10}=200_8$	$256_{10}=400_8$
Data Words/Track	$1536_{10}=3000_8$	$3072_{10}=6000_8$
Data Words/Surface	$307{,}200_{10}$	$614{,}400_{10}$
Data Words/Drive	$614{,}400_{10}$	$1{,}228{,}800_{10}$
Bit Density	≈1100 bpi	≈2200 bpi

Recording Method:	Double Frequency
Data Transfer Path:	Unibus (when the RK11 is bus master, Direct Memory Access (DMA) is performed)
Priority Interrupt:	The RK11 has a priority level of BR5 and an interrupt vector address of 220

1.3.4 Timing Format

This paragraph lists the various operation times and timing features of the RK11 System.

Access Times: (All Drives)	Track to Track:	16 ms
	Average Random Move:	70 ms
	Average Rotational Delay:	20 ms
	Rotational Speed:	1500 rpm
	Maximum Move:	130 ms
Data Transfer Rate:	Low density:	22.2 μs/word
	High density:	11.1 μs/word
Seek Function Time for Head Positioning:	50 μs to 135 ms	

1.3.5 Power Requirements

This paragraph lists the power requirements pertaining to the RK11 logic and disk drive units in the RK11 System. Also listed are the model designations of the RK11 units in relation to the power supplied.

Model Designations:

Control:	RK11-CA 115V 50/60 Hz RK11-CB 230V 50/60 Hz
Drives:	RK02-XY or RK04-XY for 600K word cartridge RK03-XY or RK05-XY for 1.2 million word cartridge

X= A for 1st drive, B for 2nd drive, C for 3rd drive, D for 4th drive, E for 5th drive, F for 6th drive, H for 7th drive, J for 8th drive

Y= A 115V 50/60 Hz, B 230V 50/60 Hz

Cartridges:	RK02-KA for the 600K word cartridge RK03-KA for the 1.2 million word cartridge

RK11 Control Power Requirements:

ac Power:	Refer to the H720 description in Chapter 4
dc Power:	5A with +5V typical and less than 0.5A at -15V.

Disk Drive Power Requirements:

ac Power:	Refer to the H734 description in Chapter 4
dc Power:	At +15 Vdc ± 5%, 4A average current and 7A start-up or instantaneous current. At -15 Vdc ± 5%, 4A average current and 7A instantaneous.

1.4 RELATED DOCUMENTS

This paragraph provides a list of documents related to the RK11 System, pertaining to its use as a peripheral of the PDP-11 Computer.

Title	Number	Description
	General	
1. *PDP-11 Handbook*	Second Edition 1970	Discussion of overall system, addressing modes, and basic instruction set from a programming point of view. Some interface and installation data.
2. *Logic Handbook*	DEC, 1970	Presents functions and specifications of the M-series logic modules and accessories used in PDP-11 interfacing. Includes other types of logic produced by DEC but not used with the PDP-11.
	Hardware	
3. *Unibus Interface Manual*	DEC-11-HIAB-D	Used in conjunction with this manual. Provides detailed theory, flow, and logic descriptions of Unibus and external device logic. Discusses methods of interface construction and provides examples of typical interfaces.
4. *PDP-11/20 System*	DEC-11-HR1A-D	Introduction, general description, specifications of entire PDP-11/20 system. Also contains operating procedures and controls and indicators for both PDP-11 and Teletype.
5. *KA11 Processor*	DEC-11-HR2A-D	Block diagram discussion, detailed theory of operation related to flow diagrams, instruction set, module descriptions, and related logic diagrams, maintenance, and adjustments.
6. *MM11-E Core Memory*	DEC-11-HR3A-D	General discussion, detailed theory of operation, bus transactions, adjustments, maintenance aids, and logic drawings.
7. *KL11 Teletype Control*	DEC-11-HR4A-D	Theory of operation, adjustment and calibration, programming data, maintenance aids, and logic drawings.
8. *H720 Power Supply & Mounting Box*	DEC-11-HR5A-D	Power supply block diagram discussion, theory of operation, circuit diagrams. Mounting box description and specifications for all models and cabinets. Includes installation information.
9. *KY11-A Programmer's Console*	DEC-11-HR7A-D	General description, flow diagram discussion, module description, and related logic diagrams. Operation and controls and indicators covered in *PDP-11/20 System Manual.*
10. *PDP-11 Conventions*	DEC-11-HR6A-D	General maintenance, logic symbology, drawing set explanation, processor signals, product identification codes, glossary, abbreviations.
	Software	
11. *Paper Tape Software Programming Handbook*	DEC-11-GGPA-D	Detailed discussion of the PDP-11 software system used to load, dump, edit, assemble, and debug PDP-11 programs. Also includes discussion of input/output programming and the floating-point and math package.
12. *Disk Operating System Monitor Programmer's Handbook*	DEC-11-SERA-D	Detailed discussion of PDP-11 disk operating system montior software. Includes programmed requests and keyboard commands for PDP-11 disk control systems.

CHAPTER 2
PROGRAMMING

2.1 INTRODUCTION

The RK11 software interface is presented in this chapter. This includes device registers and their addresses, the interrupt process, timing considerations, and data format. Finally, programming examples are provided to illustrate software interface functions as well as basic RK11 hardware operation.

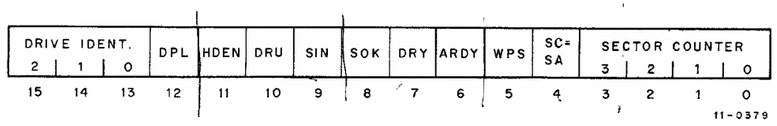
2.2 DEVICE REGISTERS AND ADDRESSES

All RK11 software control is done with the eight device registers. These registers are assigned memory addresses and can be read or written into (with the exceptions noted) using instructions that refer to the respective register addresses. The eight device registers, their bit assignments, and memory addresses are listed below. Unassigned and write only bits are always read as zeros. Loading unassigned or read only bits has no affect on the bit. The INIT signal refers to the initialization signal issued by the processor.

DRIVE STATUS REGISTER (RKDS) Address = 777400

NOTE

This register is a read only register and contains the selected drive status and current sector address.



Bit	Designation	Description and Operation
00–03	Sector Counter (SC)	These bits give the current sector address of the selected drive. This Sector Counter will work for any disk cartridge with up to 16_{10} sectors. Sector address 00 is defined as the sector that follows the sector containing the index pulse. This is an important consideration when using the R/W ALL mode of operation.
04	Sector Counter Equals Sector Address (SC=SA)	This bit indicates that the disk heads are currently positioned over the disk address currently held in the Sector Address (bits 00–03) portion of the RKDA. This address equals the Sector Counter value (bits 00–03) of the RKDS.
05	Write Protect Status (WPS)	This bit sets when the selected disk is in the Write Protected mode.
06	Access Ready (ARDY)	This bit indicates that the selected drive head mechanism is not in motion and the drive is ready to accept a new function.
07	Drive Ready (DRY)	This bit indicates that the selected disk drive complies with the following conditions: *a.* properly supplied with power *b.* loaded with a disk cartridge *c.* the disk drive door is closed *d.* the LOAD/RUN switch is in the RUN position *e.* the disk is rotating at the proper speed (must be within 99% of 1500 rpm) *f.* the heads are properly loaded *g.* the disk is not in a DRU (bit 10 of RKDS) condition.
08	Sector Counter OK (SOK)	This bit indicates that the Sector Counter operating on the selected drive (bits 00–03 of the RKDS) is not in the process of changing and is ready for examination.
09	Seek Incomplete (SIN)	Due to some unusual condition a Seek function was not completed within 180 ms of initiation. A Drive Reset function clears this bit. This bit is normally accompanied by bit 15 of the RKER (DRE).
10	Drive Unsafe (DRU)	This bit indicates that an unusual condition has occurred in the drive and it is unable to properly perform any operations. Putting the RUN/LOAD switch in the LOAD position will reset the condition. If, on putting the RUN/LOAD switch back to the RUN position the condition reoccurs, the drive or associated power supply is inoperative and corrective maintenance procedures should be initiated. This bit is normally accompanied by bit 15 of the RKER (DRE).
11	Hi Density Disk Drive (HDEN)	This bit sets to identify the selected disk drive as an RK03 or RK05 (Hi Density) and resets to identify the selected drive as an RK02 or RK04 (Low Density).

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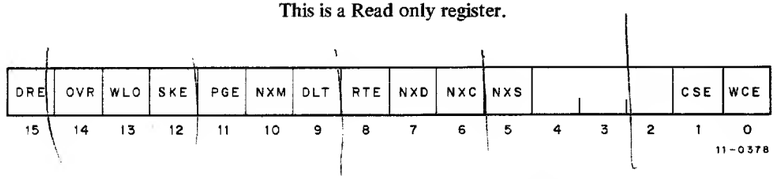
Bit	Designation	Description and Operation
12	Drive Power Low (DPL)	This bit is set when an attempt is made to initiate a new function or a function was actively in progress when the control sensed a loss of power to one of the disk drives. This bit is normally accompanied by bit 15 of the RKER (DRE) and is reset by a BUS INIT or a Control Reset function.
13–15	Identification of Drive (ID)	If an interrupt is caused as a result of a Search Complete (bit 13 of the RKCS) or a Seek Incomplete (bit 09 of the RKDS), these bits will contain the binary representation of the logical drive number that caused the interrupt.

ERRORS REGISTER (RKER) **Address = 777402**

NOTE
This is a Read only register.

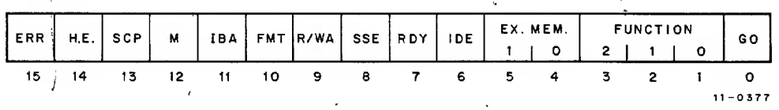


Bit	Designation	Description and Operation
00	Write Check Error (WCE)	An error was encountered during a Write Check function as a result of a faulty bit comparison between disk data and memory data. This bit clears at the initiation of a new function. This is a soft error condition.
01	Checksum Error (CSE)	This bit is set while performing a Read Check or Read function as a result of a faulty recalculation of the checksum. Cleared at the initiation of any new function and is a soft error condition.
02–04	Unused	

The remaining bits of the RKER are all hard errors. They are cleared only by a BUS INIT or a Control Reset function.

05	Non Existent Sector (NXS)	An attempt was made to initiate a transfer to a sector larger than 13_8.
06	Non Existent Cylinder (NXC)	An attempt was made to initiate a transfer to a cylinder larger than 312_8.
07	Non Existent Disk (NXD)	An attempt was made to initiate a function on a nonexistent drive.
08	Read Timing Error (RTE)	Two or more consecutive read clock pulses were dropped by the disk drive.
09	Data Late (DLT)	Sets when an NPR sequence is initiated before the previous one has completed.
10	Non Existent Memory (NXM)	Sets if memory does not respond with a SSYN within 10 μs of the time when the RK11 becomes bus master during a DATI or DATO NPR sequence. Because of the speed of the RK03 and RK05 disk drives, it is likely that if a NXM does occur it will be accompanied by a DLT error (bit 07 of the RKER).
11	Programming Error (PCE)	The Read/Write A bit (bit 09 of RKCS) or the FMT bit (bit 10 of RKCS) was set while initiating some function other than a Read or Write.
12	Seek Error (SKE)	This bit is set if the disk head mechanism is not properly positioned while executing a normal Read, Write, Read Check, or Write Check function.
13	Write Lockout Violation (WLO)	Sets if an attempt is made to write on a disk which is currently being write protected.
14	Overrun (OVR)	During a Read, Write, Read Check, or Write Check function, operations on sector 13_8, surface 1 of cylinder address 3128 were finished and the RKWC has not yet overflowed. This is essentially an attempt to overflow out of a disk drive.
15	Drive Error (DRE)	Sets when an attempt is made to initiate a function, or a function is actively in progress, while the selected drive is not ready, is in some error condition, or if one of the drives in the system senses a loss of either ac or dc power. If this bit is found to be set, the RKDS should immediately be referenced to discover the cause of this condition.

CONTROL STATUS REGISTER (RKCS) **Address = 777404**



Bit	Designation	Description and Operation
00	Go (GO) Read/Write	This bit is loaded by the operator. Loading this bit causes the control to carry out the function contained in bits 01 through 03 of the RKCS (function register). This bit remains set until the control actually begins to respond to the GO command. The period of time may be from 5 μs to 3.3 ms, depending on the current operation of the selected disk drive to protect the header area of the sector.

(continued on next page)

Bit	Designation	Description and Operation
01–03	Function (FR0, (FR1, FR2) Read/Write	The function bits or function register indicate the binary representation of the function to be performed by the control when a GO command is given. The binary coding for each of the eight functions is given in the following table. A description of each function is given in Chapter 1. The function register is loaded by the program and is cleared by BUS INIT. The function register retains the function until altered by the program or cleared, thus enabling the user to continue from a soft error condition with a GO command.

FR2	FR1	FR0	Octal Code	Operation
0	0	0	0	Control Reset
0	0	1	I	Write
0	I	0	2	Read
0	I	1	3	Write Check
1	0	0	4	Seek
1	0	I	5	Read Check
1	1	0	6	Drive Reset
1	I	I	7	Write Lock

04, 05	Memory Extension (MEX) Read/Write	These two bits are reserved for extended bus addresses used in conjunction with the RKBA. These bits make up a two bit counter that increments each time the RKBA overflows. A bus DATO to these bits overrides any RKBA overflow. These bits are loaded by the program and cleared by BUS INIT.

NOTE

The extended memory bits (RKCS bits 4–5) are intended for systems equipped with the KT11-A option, a memory larger than 32K words, and will cause the non-existent memory bit (RKER bit 10) to be set if sequenced into by the RKBA or selected by the program, when the system has 32K words or less.

06	Interrupt on Done Enable (IDE) Read/Write	When IDE is set the control issues a bus request and interrupt to vector address 220 if: a function has completed its activity, a hard error is encountered, or a soft error is encountered and bit 08 of the RKCS (SSE) is set. Bit 06 is set under program control. An interrupt will also occur if this bit is loaded without loading the GO bit and bit 07 RKCS (RDY) is set.
07	Control Ready (RDY) Read Only	Indicates that the control is ready to perform a function. Cleared as GO bit is set. Is set by INIT or a hard error condition, or the termination of a function.
08	Stop on Soft Error (SSE) Read/Write	This bit is under program control. If a soft error is encountered when this bit is set: all control action will stop at the end of the current sector if bit 06 (IDE) is reset. or all control action will stop and a bus request will occur at the end of the current sector if bit 06 (IDE) is set.
09	Read/Write All (R/W A) Read/Write	This bit is a program-controlled bit that must be used in conjunction with a Read or Write function only. When the drive heads are at the desired sector location, the read amplifiers or the write drivers are turned on and every 16-bit word is transferred to or from memory until RKWC overflows. If RKWC has not overflowed in one disk revolution, the control will not go to the next surface or next cylinder, but just wrap itself until RKWC does overflow. In this mode there is no hardware check of head positioning and RKDA does not increment until the end of the transfer. This mode of operation is used to simulate formats to be written or read on controls other than RK11's.

NOTE

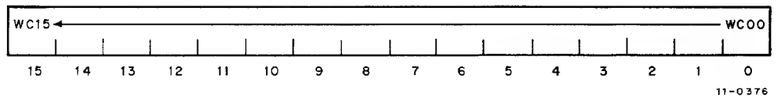
To simulate another format the programmer will have to thoroughly understand the alien format and carefully construct its sync area, all data, and any checking codes through software, keeping in mind that the control reads and writes data on the disk's least significant bit first. An IBM type 2315 disk cartridge with any number of sectors up to 16_{10} may be used in this mode.

10	Format (FMT) Read/Write	This bit is under program control and must be used only in conjunction with normal Read and Write functions. This mode is used to format a new disk pack or to reformat any sector that may have been erased due to control or drive failure. In the Format mode, the normal Write operation is altered only in that the servo positioner is not checked for proper position before the Write operation. Under a normal Write operation the header is rewritten each time the associated sector is written. The Read operation is altered in that only one word is transferred to memory per sector: the header word. Therefor, a 3-word Read function in the Format mode will transfer 3 contiguous header words from 3 continuous sectors to 3 consecutive memory locations for software checking.
11	Inhibit Incrementing the RKBA (IBA) Read/Write	This bit is set under program control and inhibits the RKBA from incrementing during a normal transfer function. This allows data transfer to or from the same memory location throughout the entire transfer operation.
12	Maintenance Mode (MAINT) Read/Write	This bit is set under program control and will inhibit any signals from being transmitted to or from any disk drive and will permit diskless operation of the RK11. This bit is used in conjunction with RKMR shown in this section.
13	Search Complete (SCP) Read Only	This bit signifies that the previous interrupt was the result of some previous Seek or Drive Reset function. This bit is cleared at the initiation of any new function.

(continued on next page)

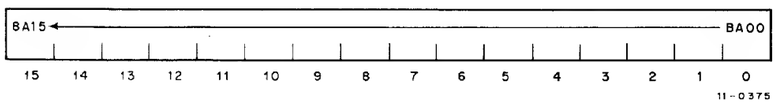
Bit	Designation	Description and Operation
14	Hard Error (HE) Read Only	Sets when any of bits 05–15 of the RKER are set. This bit stops all control action and the processor reaction is dictated by bit 06 (IDE) of the RKCS. This bit, along with bits 05–12 of the RKER, is cleared by INIT or a Control Reset function.
15	Error (ERR) Read Only	Sets when any bit of the RKER sets. Processor reaction is dictated by bit 06 (IDE) and bit 08 (SSE) of the RKCS. This bit is cleared if all the bits in the RKER are cleared and if bit 14 of the RKCS is cleared.

WORD COUNT REGISTER (RKWC) Address = 777406



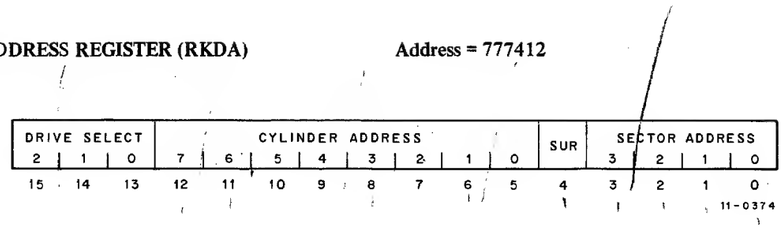
Bit	Designation	Description and Operation
00–15	WC00–WC15 Read/Write	The bits in this register contain the 2's complement of the total number of words to be affected or transferred by a given function. The register increments by one after each word transfer. When the register overflows (all WC bits go to zero) the transfer is complete and RK11 operation is terminated at the end of the present disk sector. However, only the number of words sepcified in the RKWC are transferred.

CURRENT BUS ADDRESS REGISTER (RKBA) Address = 777410



Bit	Designation	Description and Operation
00–15	BA00–BA15 Read/Write	The bits in this register contain the bus address to or from which data will be transferred. The register is incremented by two at the end of each transfer. If the system has extended memory, then the RKBA will overflow to the EX MEM (bits 04 and 05) of the RKCS to reflect the extended bus addresses. If, however, there is no memory extension an overflow with no RKWC overflow will cause an NXM error (bit 10) in the RKER.

DISK ADDRESS REGISTER (RKDA) Address = 777412

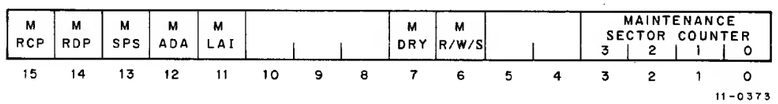


NOTE

All RKDA bits are loaded from the bus data lines only in RK11 READY state, and cleared by BUS INIT and Control Reset. The RKDA is incremented automatically at the end of each disk sector.

Bit	Designation	Description and Operation
00–03	Sector Address (SC)	Binary representation of the disk sector to be addressed for the next function.
04	Surface (SUR)	When active the lower disk head is enabled and operation is performed on the lower surface. When inactive the upper disk head is enabled.
05–12	Cylinder Address (CYL ADD)	Binary representation of the cylinder address currently being selected. The largest valid address or number for the cylinder address is 312_8.
13–15	Drive Select (DR SEL)	These bits contain the binary representation of the logical drive number currently being selected.

MAINTENANCE REGISTER (RKMR) Address = 777414



NOTE

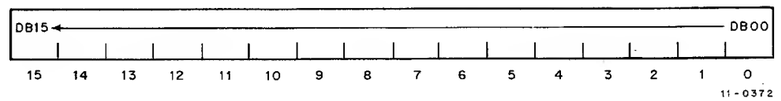
This register is loaded from the bus data lines and is enabled for RK11 diskless debugging operations by the setting of bit 12 of the RKCS (M). This register simulates by program control the disk drive signals to the RK11 Control.

Bit	Designation	Description and Operation
00–03	Maintenance Sector Counter (MAINT SEC CNTR) Read/Write	Loading these bits will simulate the sector counter lines otherwise being received from the selected disk. This bit configuration will appear in bits 00–03 of the RKDS.
04–05	Unused	

(continued on next page)

Bit	Designation	Description and Operation
06	Maintenance Ready to Read/Write or Seek (MAINT R/W/S RDY) Read/Write	Loading this bit will simulate the R/W/S RDY condition otherwise being received from a selected disk drive and will appear in bit 06 of the RKDS, Access Ready (ARDY). This bit indicates that the disk heads are in motion when reset. Therefore, when attempting to simulate a disk in a static condition, this bit must be set.
07	Maintenance Drive Ready (MAINT DRY) Read/Write	Loading this bit will simulate the DRY condition otherwise being received from a selected disk drive and will appear in bit 07 of the RKDS (DRY).
08–10	Unused	
11	Maintenance Logical Address Interlock (MLAI) Write Only	Loading this bit simulates the disk logical address interlock pulse otherwise being received from the selected disk drive. Normally, the pulse is received from a disk drive if an attempt is made to issue a function on some cylinder address larger than 312_8. This bit allows the program to simulate an NXD condition (bit 07 of the RKER).
12	Maintenance Address Acknowledge (MADA) Write Only	Loading this bit simulates an ADDRESS ACKNOWLEDGE pulse otherwise being received from the selected disk drive. This pulse is received after initiation of any Seek, Read, Write, Read Check, or Write Check function to indicate that the disk drive has accepted the cylinder address from the RKDA. In essence, this bit allows the simulation of a head movement sequence.
13	Maintenance Sector Pulse (MSPS) Write Only	Loading this bit simulates the SECTOR pulse otherwise being received from the selected disk drive. It defines sector boundaries and should increment the sector counter (bits 00–03 of the RKDS).
14	Maintenance Read Data Pulse (MRDP) Write Only	Loading this bit simulates a READ DATA pulse otherwise being received from the selected disk drive. This pulse comes between READ CLOCK pulses and indicates that a 1 has been read from the disk drive. If no READ DATA pulse occurs between consecutive READ CLOCK pulses a 0 has been read from the disk.
15	Maintenance Read Clock Pulse (MRCP) Read Only	Loading this bit simulates a READ CLOCK pulse that would otherwise be received from the selected disk drive. This pulse defines the bit cell boundaries of data being received from the disk.

DATA BUFFER REGISTER (RKDB) **Address = 777416**



Bit	Designation	Description and Operation
00–15	DB00–DB15 Read Only	The bits of this register work as a general data handler in that all information transferred between the control and the disk drive must pass through this register. It is loaded from the bus only while the RK11 is bus master during an NPR sequence.

2.3 INTERRUPT PROCESS

For any interrupt condition to cause an interrupt, IDE must be set in the RKCS. The RK11 will interrupt on any one of six conditions. These conditions are: the presence of a hard error (HE set in the RKCS); the presence of a soft error with the program-controlled SSE (stop on soft error) set when the major state register (MSR) is cleared; WC OVF (word count overflow); set at the end of a sector indicating the end of a data block transfer; the presence of Seek Started which indicates that a drive has initiated a Seek or Drive Reset freeing the RK11 logic which can now pole if desired; the initiation of Write Protect on a disk drive; and the setting of INT SCH CMP (interrupt search complete) stating that a poll has been completed. INT SCH CMP will not appear unless IDE is set in the RKCS prior to polling. This is due to the fact that the poll cannot be initiated unless IDE is set.

Because of the RK11 format structure, any interruption of a Write sequence cannot be tolerated until the end of the sector because this would result in, essentially, an unformatted disk. Therefore, any outside intervention is inhibited until the end of the current disk drive sector, which includes the Control Reset function and the processor or BUS INIT signals. Therefore, all those functions, such as Control Reset, Seek, and Write Lock, which normally take only a few microseconds to initiate, can actually take up to 3.3 ms if initiated during a Write function. For this reason the Seek and Write Lock functions will cause an interrupt (if IDE is set in the RKCS) as soon as the function has been successfully initiated. The Control Reset function, which cannot cause an interrupt under any circumstance can, therefore, take up to 3.3 ms to complete. To determine if this function is complete, a monitor of the Ready bit of the RKCS must be used in the software. It is set when any function is complete.

2.4 TIMING CONSIDERATIONS

The RK11 timing considerations pertain to performance of overlapped Seek or Drive Reset functions; that is, the initiation of another Seek or Drive Reset function on another drive as soon as one drive has started the previous Seek or Drive Reset. This can be done for up to eight Seeks or Drive Resets, one for each disk drive. The hardware pole logic interrupts the processor as each Seek or Drive Reset is poled and found to have completed each drive. After initiating a Seek or Drive Reset function, an interrupt occurs if IDE is set in the RKCS indicating that the function has been accepted and execution has begun. This may take from 50 μs to 350 μs. The actual Seek, however, may take as long as 50 μs to 135 ms, after which a second or Search Complete interrupt occurs, if IDE

is set. In the time between these two events the selected disk drive is busy moving its heads, but the control is free to perform any function on any other available disk drive, including another Seek or Drive Reset. It should be noted, however, that once a disk has begun to move its heads, the only function that can stop it is a Drive Reset. An attempt to perform any other function on a drive whose heads are in motion will result in a hard error condition. It should be noted that all Read, Write, Read Check, and Write Check functions employ the Seek operation. This allows the user of a single-disk system to completely forget about the Seek function and initiate transfer functions directly. Also, when using the transfer function, as would be the case in a single disk system or when desired in any system configuration, the hardware poll is not incorporated for use and will not cause an interrupt to indicate a completed Seek.

2.5 DATA FORMAT

Data is stored on the disk cartridge in groups of 12 sectors per cylinder. Each sector contains either 128 or 256 words depending on whether the disk is low or high density, respectively. The twelve disk sectors are defined by physical sector marks that are picked up by the drive logic and transmitted to the RK11 Control. Also, another similar physical mark called an index mark defines the starting point for the sequence of sectors within a cylinder. Each sector on each disk is formatted identically. The sector format consists of five parts: Preamble, Header, Data, Checksum, and Postamble. These sector areas correspond to the major states of the MSR logic in the RK11 Control. The MSR Idle major state only means that the RK11 operation is not taking place in any of the defined sector areas and is, therefore, either a non-data transfer operation, except for the Read Check, or the clear state of the RK11 logic.

The Preamble and Postamble sector areas or major states are guard areas designated to protect the Header, Data, and Checksum areas in the sector. These guard areas protect the sector against overwriting from another sector and allow the drive heads room to sync in on the sector information. The Preamble guard area lasts for an RK11 internal word count (see Paragraph 3.2.9) of 6_8 words for a low-density disk and for an internal word count of 15_8 words for a high-density disk. The Postamble guard area lasts for an internal word count of 4 words. These word count specifications of the guard areas are counts of 16-bit data words being transferred.

The Header area of a sector follows the sync bit and 8 bits of address information. This address information is the cylinder address of the cylinder in which the respective sector is located. The sync bit of the Header is used to sync up the RK11 Control logic for sequencing a data transfer operation. This Header area is always read and checked by the RK11 Adder logic with the respective value contained in the RKDA to ensure proper cylinder location at the initiation of a data transfer function. The Write function always re-writes the Header from the RKDA onto the disk. Also, the Header identifies the cylinder that the heads are positioned at to the drive address logic.

The Data sector area is where 128 words for the low-density drive or 256 words for the high-density drive are serially formatted bit by bit for the entire area. These data words are serially formatted for the whole sector and the 16-bit boundary for each word is monitored by the bit counter logic in the RK11 Control (see Paragraph 3.2.9).

The Checksum area of the sector is the 16-bit sum of each data word of the sector. This word maintains sector parity and is checked by the RK11 Control against the checksum value calculated in the Adder logic at the termination of a sector. This is done for a Read, Write Check, or Read Check function. For a Write function, the Checksum is calculated by the Adder logic as each word goes through the RKDB. After the last word goes through the RKDB, the calculated Checksum value is loaded into the RKDB and sequentially written on the disk following the last data word.

2.6 PROGRAMMING EXAMPLE

Program control of the RK11 Disk Control System can be accomplished by using the Disk Operating System Monitor software for the PDP-11. This system is described in the *Disk Operating System Monitor Programmer's Handbook* (DEC-11-SERA-D). Basic program control is initiated by loading the disk control registers. The control then performs the specified function and will cause an interrupt to the software routine whose starting address is in location 220 when done or when an error occurs, if IDE in the RKCS is set. Otherwise, the program may test the word count register and the error bit (RKCS) to determine completion.

The following subroutine can be used to initiate Transfers or Seeks. The interface is as follows:

The caller builds up the following table:

```
TABLE:
DKSADR:     .WORD 0          ;ADDRESS ON THE DISK
MEMADR:     .WORD 0          ;ADDRESS IN MEMORY OF DATA
WRDCT:      .WORD 0          ;2'S COMPLEMENT WORD COUNT
FCTN:       .WORD 0          ;DESIRED FUNCTION: BITS
                             ;6 & 0, IDE & GO RESPECTIVELY,
                             ;MUST BE SET
FLGWRD:     .WORD 0          ;FLAG WORD: 0 = SEEK,
                             ;NOT 0 = DO FUNCTION
```

On return, if R1 ≠ 0 in the processor, then the function was initiated. If R1 = 0 in the processor, then it was not, because the RK11 Control was busy. Thus the following interface:

```
                             ;SET UP THE TABLE
                .
                .
                .
                MOV #TABLE, R0   ;PASS THE POINTER
                JSR PC, SUBR     ;CALL SUBR
                TST R1           ;WAS THE FUNCTION STARTED?
                BEQ NOGO         ;NO – BRANCH
GO:                              ;YES IT WAS
                .
                .
                .
NO GO:
                .
                .
                .
RKDS = 177400    ;DRIVE STATUS REGISTER
RKER = 177402    ;ERROR REGISTER
RKCS = 177404    ;RK11 CONTROL STATUS REGISTER
RKWC = 177406    ;WORD COUNT REGISTER
RKBA = 177410    ;BUS ADDRESS REGISTER
RKDA = 177412    ;DISK ADDRESS REGISTER
PS   = 177776    ;PROCESSOR STATUS REGISTER
```

(continued on next page)

```
SUBR:   MOV #RKDA, R2       ;POINT TO HIGH RK REGISTER
        MOV #PS, R3
        MOV @R3,-(R6)       ;SAVE OLD STATUS
        CLR R1              ;PREPARE THE FAILURE CODE
        MOVB #240, @R3      ;RAISE TO LEVEL 5
        TSTB @#RKCS         ;IS THE RK11 CONTROL BUSY
        BPL SUB10           ;YES – BRANCH
        MOV (R0)+, @R2      ;SET DISK ADDRESS
        MOV (R0)+, -(R2)    ;SET DATA ADDRESS
        MOV (R0)+, -(R2)    ;SET WORD COUNT
        MOV (R0)+, R1       ;GET THE FUNCTION
        TST @R0             ;IS A SEEK REQUESTED?
        BNE SUB05           ;NO – BRANCH
        MOV #111, R1        ;SET TO SEEK (IDE & GO TO)
SUB05:  MOV R1, -(R2)       ;GO
SUB10:  MOV (R6)+, @R3      ;RESTORE ORIGINAL STATUS
        RTS PC              ;RETURN TO CALLER
```

CHAPTER 3
DETAILED DESCRIPTION OF THE RK11-C

3.1 INTRODUCTION

The detailed description of the RK11 Control consists of discussions of all control logic, logic functions, and control operations. This discussion is divided into five functional areas: RK11 Control Logic, Non-Data Transfer Logic, Data Transfer Logic, Error Detection Logic, and Maintenance Mode Logic. Detailed description of a disk drive used with the RK11 Control in a particular instance is found in the manual supplied with the RK11 System.

The RK11 Control Logic consists of RK11 initialization, bus receiver and driver logic, cable receiver and driver logic, internal bus, selection logic (register and disk), NPR logic, interrupt logic, basic timing logic, bit counter and internal word count logic, function register logic, disk addressing logic, word count logic, and the bus address or current memory address logic.

The non-data transfer logic consists of the Seek function logic, hardware pole logic, Drive Reset function logic, Control Reset function logic, and Write Lock function logic.

The data transfer logic consists of the major state register (MSR) and control logic, the Adder and Adder control logic, data serial buffer (DSB) logic, RKDB, data paths, and RKDB control logic, Write function logic, Read function logic, Read Check function logic, Write Check function logic, Read/Write All (R/W A) mode logic, and the Format mode logic.

The error detection logic discusses the generation of error interrupts to the processor and references the definitions of the RK11 Control error conditions.

The maintenance mode logic discusses the logic used to establish RK11 maintenance mode operation. A description is included of how the maintenance logic puts the RK11 logic into a position where the programmer can generate simulations of disk drive signals.

3.2 RK11 CONTROL LOGIC

The following paragraphs describe the various RK11 control functions that establish the primary functions performed by the RK11 Disk Control System.

3.2.1 RK11 Initialization

Initializing the RK11 is accomplished by clearing the registers and many of the flip-flops before an RK11 function. This operation is keyed by the BUS INIT signal off the Unibus which is inverted to the RK11 INIT signal. INIT is used to clear many of the RK11 flip-flops and register bits. It also generates GEN CLR which independently initializes much of the RK11 control logic (see engineering drawing D-BS-RK11-C-02). The T1 pulse also generates GEN CLR. GEN CLR is initiated at the beginning of a transfer function and generates CLR MSR, which clears the write gate (WT GATE) and the read gate (RD GATE). CLR MSR is generated at every new sector (NEW SECT). NEW SECT is ORed with GEN CLR to clear many of the data transfer related flip-flops.

3.2.2 Unibus Receivers and Drivers

The Unibus receivers and drivers are gating circuits that send and receive bus information. The Bus D Receivers and Drivers (see engineering drawing D-BS-RK11-C-19) gate the bus data lines. The receivers gate all of the bus data lines into the RK11, inverting the signals to be logically compatible to the RK11 logic circuitry. The drivers gate the data off the internal bus (INT BUS 00 – 15) to the bus data line. The bus address lines and control lines are received in the selection and NPR logic. The control signals are gated or driven onto the bus C lines by the NPR logic. The address lines are driven onto the bus by the RKBA and RKWC.

3.2.3 Cable Receivers and Drivers

The cable receivers and drivers are gating circuits that send and receive data between the RK11 Control and the disk drive. The drivers gate all address information and control signals into the selected disk drive (see engineering drawing D-BS-RK11-C-17). The receivers gate the control and status signals of the selected disk drive to the RK11 Control and invert these signals so they are logically compatible with the RK11 logic circuitry.

3.2.4 Internal Bus

The internal bus provides an internal communication line within the RK11. The bus receives each bit of the RKDS, RKCS, RKDB, RKDA, and the RKMR (see engineering drawing D-BS-RK11-C-20). Each line of the internal bus (INT BUS 00 – 15) represents one bit of each register simultaneously. The internal bus communicates this information to the Bus D Drivers for gating onto the Unibus.

3.2.5 Selection Logic

The RK11 selection logic determines the registers addressed by the processor. Selection is accomplished by the M105 and M797 module logic shown on engineering drawing D-BS-RK11-C-11. The M105 performs address selection and the M797 performs register selection. The disk selection logic shown on engineering drawing D-BS-RK11-C-06 is also included.

The M105 Address Selector Module decodes address information from the Unibus. In the RK11, the M105 is set up, because of the V2, F1, and H1 grounding arrangement, to recognize all address lines except A01, A02, and A03. Address line A00, which is the least significant digit of the address, is recognized by the M105 to determine a byte or word operation. The exclusion of address lines A01, A02, and A03 in the M105 allows the logic to generate the signal ADD DEC * MSYN L to the M797 for eight possible addresses. This arrangement occurs

because the M105 can select only four addresses, while the RK11 contains eight addressable registers. Address lines A01, A02, and A03 represent the least significant octal bit of the register address whose value is recognized in the M797 Register Selection Module. The M797 is discussed in the following paragraph. The jumpers on the M105 determine the eight possible addresses that will enable the ADD DEC * MSYN L signal. The RK11 jumpers are set to recognize addresses 777400 through 777416. Although these addresses have been selected by DEC as the standard assignments for the RK11 registers, the customer can change the jumper arrangement to any addresses desired. Finally, the M105 gates the BUS C00 and BUS C01 signals to generate IN and OUT signals, which determine whether a register is reading or writing, respectively.

The M797 Register Selection Module determines which registers have been selected by the processor and whether these registers are reading or writing. The input signal ADD DEC * MSYN L from the M105 is present when a valid address up to the least significant octal digit has been recognized by the M105 with MSYN. The input OUT signals gate with ADD DEC * MSYN L to initiate the M797 decoders for the generation of register LO EN and HI EN signals for writing or reading of these registers, respectively. The A01, A02, and A03 address line signals come off the bus receivers and determine which of the eight registers have been selected. The decoder then generates the register HI EN and LO EN signals for the respective register addressed. Finally, M797 generates START XFER TIMING when a valid address is received through the decoder and initiates the LOAD REG signal for a DATO operation.

The disk selection logic selects the disk drive to be used for the upcoming RK11 operation. The G740 Disk Selection Module determines if a valid disk has been selected. Up to eight disks can be recognized individually on the G740. The selected disk value is input to the G740 to be checked for validity. The disk is selected in bits 13 through 15 of the RKDA register or in bits 13 through 15 of the RKDS during the hardware poll. This disk selection circuitry generates the disk select signals that are input to the G740, where the jumper arrangement determines the selected disk's validity. The G740 jumpers are connected to account for or enable any of the disks in a particular RK11-controlled disk system. According to the number of disks used, the G740 generates the appropriate SELECT signals, A to a possible J from 0 to a possible 7 disks, respectively. These SELECT outputs (A through J) are hardwired to disk 0 through 7, respectively; the G740 allows any logical unit to be designated to them.

3.2.6 NPR (Non-Processor Request) Logic

The NPR operation is initiated when the RK11 wants to establish a communications channel and perform a data transfer with memory. To establish a communications channel, the RK11 must obtain control of the Unibus and become bus master. The following discussion illustrates how the RK11 becomes bus master and initiates the NPR data transfer. Refer to engineering drawing D-BS-RK11-C-11 (Sheets 1 and 2) for the NPR logic.

When the RK11 desires to initiate an NPR to perform a data transfer either to or from a disk drive, the NPR flip-flop is set. This flip-flop is clocked for a Read function, Write function in the Read/Write All (R/W A) mode, or a Write Check function. For a Read function, the NPR flip-flop is clocked for each word as it is gated from the DSB to the RKDB (GATE DSB to RKDB). For a Write or Write Check function, the NPR flip-flop is clocked by RKDB to DSB, which moves each word to be written or write checked from the RKDB to the DSB. The presence of LAST WORD IN PROGRESS or LAST WORD DONE terminates all NPR clocking for a Write or Write Check function. In the R/W A mode, a Write function initially generates the clock to the NPR flip-flop when NEW FUNCTION is present. In order for the NPR flip-flop to set for each clock, the input must indicate that no hard errors are present, no stop on soft errors are present, the data transfer word count has not gone to 0 (WC OVF), and that the last NPR was completed before the new data word count could cause a clock to the NPR flip-flop (DLT = 0). DLT will set and disqualify the NPR input if the NPR is clocked when it is in the 1 state. Finally, the NPR flip-flop can be set if the RK11 is in the Format mode (FMT) (NORMAL unasserted), and in the Header major state when the header word is gated from the DSB to the RKDB during a Read function (GATE DSB → RKDB).

The NPR flip-flop is input to the M782 and, when NPR is set, M782 generates BUS NPR (providing DLT of the RKER is clear). BUS NPR requests NPR control of the bus from the processor. If the RK11 priority is such that the RK11 can be the next bus master, the processor replies with BUS NPG (Non-Processor Grant) IN. BUS NPG IN causes the M782 to generate BUS SACK back to the processor. At this point, the RK11 is set up to be the next bus master and now must wait for the present bus operation to terminate. When BUS BBSY and BUS SSYN are removed from the bus as the previous operation terminates, the RK11, with BUS NPG absent, drops BUS SACK on the bus and generates RK NPR MASTER which, in turn, generates RK BUS MASTER. RK NPR MASTER inputs the M796 which gates the data (if Read only) and address lines to the bus and enables the bus control lines (BUS C01 and C00). For a Write or Write Check function, data is moved by the generation of DATA STR 1 in the M796. This signal clears the RKDB and generates LOAD RKDB, which enables the loading of the RKDB for each NPR. The 0 → NPR signal, which clears the NPR flip-flop, is also generated in the M796. When BUS SSYN returns from the processor and is input to the M796 and M782 as INT BUS SSYN, the data has been transferred. This transfer action causes M796 to drop BUS MSYN and M782 to drop BUS BBSY. The generation of 0 → NPR increments the RKBA and the RKWC for the next word to be transferred.

In RK11 operation, if INT BUS SSYN does not occur 10 μs after BUS MSYN is asserted by the RK11, the M796 generates NXM (1) H, which sets the NXM bit in the RKER. This indicates that a nonexistent memory location was addressed in core and, in turn, ERR is set in the RKCS. A detailed description of the M782 and M796 Modules is found in the *Unibus Interface Manual* (DEC-11-HIAB-D).

3.2.7 Interrupt Logic

For an interrupt to occur under any condition, the interrupt done enable bit (IDE) in the RKCS must be set; otherwise, any condition that causes an interrupt will not be honored. The IDE bit is set under program control. With IDE set, the following RK11 interrupt conditions will initiate an interrupt to the processor: INT SCH CMP (internal search complete) is set in the hardware poll logic indicating that a Seek or Drive Reset has been completed by the specified disk drive; a Seek function has been initiated and acknowledged by a disk drive and, therefore, frees the RK11 to perform another operation (Seek Started); a function is initiated to Write Protect a disk drive (WT PROTECT); a data transfer function has reached the end of a disk sector and word count has overflowed (WC OVF); a soft error has occurred with the stop on soft error (SSE) set in the RKCS (is set by program control); or the occurrence of a hard error condition. All the above conditions, except INT SCH CMP, are reflected by the signal 1 → XFC generated in the logic shown on engineering drawing D-BS-RK11-C-11, Sheet 2.

The logic shown on engineering drawing D-BS-RK11-C-11, Sheet 1, includes the logic that initiates an interrupt in the M782 Interrupt Control Module. The RDY INT (Ready Interrupt) flip-flop, with RDY in the RKCS already set, is clocked by program setting of IDE in the RKCS. This condition direct sets the INT XFC (internal transfer complete) flip-flop. This flip-flop can also be set when 1 → XFC appears to clock it for any of the interrupt conditions provided IDE is set. The state of the INT XFC flip-flop is ORed with the interrupt condition INT SCH CMP to generate INT REQ (interrupt request), which is input to the M782. INT SCH CMP (internal search complete) is the interrupt condition which states that the hardware poll of previous Seek functions or Drive Reset functions for particular disk drives is complete. Asserting INT REQ to the M782 causes the M782 to generate BR OUT (bus request) onto the bus. The bus reply of BG IN (bus grant), if the RK11 priority (BR5) is next in line for bus control, generates BUS SACK from the M782 to the bus. When the bus drops BUS SSYN and BUS BBSY, terminating previous bus operation, M782 generates BUS BBSY onto the bus; also, RK INT MASTER is generated, which gates the interrupt vector address onto the bus data lines; and BUS INTR

is generated, which initiates the processor's interrupt service routine. When BUS SSYN returns, generating INT BUS SSYN onto the M782, INT DONE is generated. This relinquishes control of the bus and clears M782, the RDY INT flip-flop, INT XFC flip-flop, and the INT SCH CMP flip-flop.

3.2.8 Basic Timing

The basic timing logic for the RK11 timing signals is shown on engineering drawing D-BS-RK11-C-02. The signals generated in this logic are used throughout the RK11 for timing, delays, and clocking.

The signals CLK LE (clock leading edge) and CLK TE (clock trailing edge) are 100-ns pulses generated by either STD RD CLK (standard read clock) from the disk drive or WT CLK (1) (write clock) in the RK11 (see Paragraph 4.5.5). STD SEC PLS (standard sector pulse) is generated by DISK SEC PLS, which rises because of the physical sector mark on the disk. STD SEC PLS is generated when POLL is unasserted or by the assimilated maintenance sector pulse (MAINT SEC PLS). This sector pulse signal tells the RK11 each time a new sector is coming under the head.

Whenever the heads change to another cylinder or operation is changed from one head to another, due to changing from one disk surface to another, the heads need time to settle and allow the head amplifiers to bias properly. This also applies for polling when POLL is asserted and when the Write Gate is set. A 100-μs delay is provided to allow the heads to settle, generating HEAD SETTLE DLY. This signal is asserted when the Write Gate is set (WT GATE (1)), when the surface is changed or the cylinder address is incremented (COUNT DA (1)), when the addressing logic of the disk is not ready (R/W/S RDY is unasserted), or when POLL is asserted.

At the initiation of any RK11 operation, the logic is initialized due to GO being set in the RKCS. When a new sector is reached (STD SEC PLS is asserted) under a GO condition (CONTROL RDY (0)), the signal NEW SECTOR is generated. Therefore, NEW SECTOR is generated each time a standard sector pulse is located during normal RK11 operation. However, in the Read/Write All (R/W A) mode of RK11 operation, the generation of NEW SECTOR is inhibited when either the Read or Write Gate flip-flops are set. This frees any data transfer operation from the RK11 disk format in order for other formats to be simulated in the RK11, which is the purpose of the Read/Write All mode of operation. Setting GO inputs a 4-μs one-shot that generates GEN CLR. GEN CLR is also generated in this network by INIT from the bus. The previous conditions that generated GEN CLR also generate two timing signals, T1 and T2, with T2 coming 1 μs after T1 goes low. These signals initiate the RK11 logic for the function about to be performed. Generating NEW SECTOR also generates clocking signals for the Read and Write Gate flip-flops, with 1 → WT GATE being an 11-μs pulse, 1 → RD GATE being an 85-μs pulse.

The STD RD CLK and STD RD DATA signals are generated by the disk read data and read clock signals off the Read amplifiers. The read clock signal is a 350-ns pulse; the read data signal is a 100-ns pulse. The maintenance assimilation of these disk read logic signals is done in the RK11 maintenance mode.

Any function other than Control Reset, with no hard error present (HE (0)) and T2 timing out, generates the signal NEW FUNCTION through a 1-μs one-shot. When GO is set, causing the delayed assertion of T2, NEW FUNCTION is asserted indicating that GO has initiated a new RK11 function. The assertion of T2 for a Control Reset function initiates CONTROL CLEAR, which clears all RK11 logic.

3.2.9 Bit Counter and Internal Word Count Logic

The bit counter and internal word count logic monitor each bit of every word and every bit within any sector on the disk. Counting all bits and words of a sector tells the RK11 control logic when it reaches the last bit of every word and the last word of every sector. Actually, this count is for each major state, and primarily, the Data major state. This bit and word counting is done by an M236 whose information is interpreted by the associated logic (see engineering drawing D-BS-RK11-C-09).

The M236 Bit and Internal Word Counter contains a clear and clock input. The clear input is initiated by COUNT MSR, GEN CLR, or NEW SECT. COUNT MSR clears the M236 as the RK11 changes major states. GEN CLR is initiated at the start of RK11 operations; NEW SECT clears the M236 each time a new sector is reached. NEW SECT is generated by STD SEC PLS (standard sector pulse), which is asserted by the physical sector marks on the disk. The clock input to the M236 consists of ACTIVE and CLK LE. The signal ACTIVE provides assurance that the RK11 is operational. In other words, the RK11 is in any of the major states except IDLE and the RDY bit of the RKCS is clear. The signal CLK LE provides a 100-ns clocking pulse generated from either the read or write clock. This signal clocks each bit time in a sector to increment the M236 Counter. Each time CLK LE is asserted M236 increments. Bits BC 00 through BC 03 count up to 17 octal bits or 16 decimal bits (standard PDP-11 word length). Every time the BC bits overflow they increment the internal word count (IWC). The bits IWC 00 through IWC 07 count up to 400 octal words or 256 decimal words (the number of words per high-density sector). In addition, the M236 contains an input that controls the counter for a high- or low-density disk. The signal LO DEN is asserted for a low-density disk and unasserted for a high-density disk. For a high-density disk, the word count per sector is 400 octal; for a low-density disk, it is 200 octal. Asserting LO DEN causes the IWC bits of the M236 to overflow at a count of 200 octal. The signal LO DEN reflects the state of the HDEN bit of the RKDS. When HDEN is clear, LO DEN is asserted and IWC overflows at 200 octal. When HDEN is set, LO DEN is unasserted and IWC overflows at 400 octal.

Each time the BC count is 17 octal the signal BC=17 * CLK LE is generated. This signal sets the LAST BIT flip-flop which tells the RK11 logic that the last bit of a word has been reached. When IWC count reaches 400 octal, the signal LAST WORD IN PROGRESS is generated. This signal, when the BC count is at 17 octal (BC=17 * CLK LE), generates 1 → LAST WORD DONE which sets the LAST WORD DONE flip-flop. Setting LAST BIT will, when the RK11 is in the Header, Checksum, or Postamble major state, generate COUNT MSR, which will put the logic in the Data, Postamble, or Idle major states, respectively, and clear the M236. Setting LAST WORD DONE, when the RK11 is in the Data major state, will also generate COUNT MSR and put the logic into the Checksum major state and clear the M236.

The M236 is also used to determine sync overflow in the Header major state. For a high-density disk, sync overflow (SYNC OVF) is reached at an IWC count of 15 octal. For a low-density disk, sync overflow is reached at an IWC count of 6. The signal SYNC OVF is generated in either case and is used in the MSR control to direct-set the END OF SYNC flip-flop.

3.2.10 Function Register

The function register consists of bits 01 through 03 of the RKCS that are program controlled. The three bits of the function register provide an octal code for any one of the eight RK11 functions. The octal code for each function is shown in Chapter 2. The function register bits of the RKCS (engineering drawing D-BS-RK11-C-03) are loaded off the bus data lines (BUS D 01 through BUS D 03) by the signal GATE BUS → RKCS LO which is generated by the RKCS control by the register selection signals BUS → RKCS LO EN and LOAD REG. LOAD REG is also generated by the register selection logic when INT BUS SSYN is unasserted. When the GO bit in the RKCS is set, the contents of the function register are loaded into the INT FUN (internal function) register in the MSR logic (engineering drawing D-BS-RK11-C-04) by the signal T1. The INT FUN 0 through INT FUN 2 bits represent the same octal function coding as the RKCS function register and are input to the M161 function decoder where, according to the function represented in the INT FUN bits, the function signal is asserted. The GO bit of the RKCS is cleared either by a new function or when the RDY bit is set in the RKCS. The function code is retained in the RKCS function register and will be re-asserted when the GO bit is set, unless a new function has been loaded into the function register. In this case, the new function will be asserted when GO is set. The RDY bit is cleared when GO is set. Any interrupt condition except INT SCH CMP will set RDY, if it is not already set.

3.2.11 Disk Addressing Logic

The disk addressing logic consists of the Disk Address Register (RKDA) and its associated control logic (see engineering drawing D-BS-RK11-C-08). This register designates the disk, cylinder address, surface (upper or lower), and sector address to be operated on by the RK11. Disk addressing logic provides loading signals, incrementing signals, and status signals for the RKDA.

Initially, the RKDA is loaded off the bus data lines, with the disk address information that is gated into the register by GATE BUS → RKDA HI for bits 08 through 15 and by GATE BUS → RKDA LO for bits 00 through 07. Bits 00 through 03 provide the sector address, bit 04 designates the surface (set for lower surface head enable), bits 05 through 12 provide the cylinder address, and bits 13 through 15 select the disk drive. The sector address portion of the RKDA is compared with the sector counter of the RKDS to recognize when the drive heads have reached the sector called for by the RKDA. The sector counter and sector address are a count of the sectors on each surface of a cylinder referenced by the index mark and keyed by the sector mark. The cylinder address is the value of the header in each sector of a cylinder. The drive select bits of the RKDA provide the disk code to the disk selection logic.

During RK11 operation, the RKDA is incremented for each sector operation. At the end of each sector operated upon, the sector address is incremented by the signal SECTOR END (1). This flip-flop is part of the major state control and reflects the end of a sector. When the last sector on the disk surface is reached, the index pulse (INDX PLS) generated by the index mark on the disk sets the LAST SECTOR flip-flop. Setting LAST SECTOR and asserting SECTOR END sets the COUNT DA flip-flop. LAST SECTOR is cleared by GEN CLR or NEW SECTOR. COUNT DA increments the RKDA above the sector address portion, as well as generates CLR SA, which clears the sector address portion of the RKDA. In incrementing RKDA at bit 04, COUNT DA changes the surface that is operating on the disk. If the drive is operating on surface 0, COUNT DA sets bit 04 which changes the drive head operation. The drive now is operating on surface 1 in the same cylinder. However, if the drive is operating on surface 1, COUNT DA will overflow bit 04, which increments the cylinder address and resets the SUR bit (04). Therefore, the disk is now at the next cylinder with the head for surface 0 enabled. Incrementing SUR and the cylinder address continues (unless WC overflows) until a cylinder address of 312_8 is reached. This address generates the signal LAST CYL which, if word count has not overflowed, sets SUR, and another COUNT DA is generated, indicating an overrun error situation. This is a hard error and will cause an interrupt if IDE is set. This overrun situation illustrates that any RK11 data transfer operation must be completed within the bounds of a disk. The RKDA is cleared by INIT.

3.2.12 Word Count and Bus Address Logic

The Word Count Register (RKWC) and the Bus Address Register (RKBA) or current memory address register combine to keep track of the number of words to be transferred to or from each word's sequential bus address or location in memory. Refer to engineering drawing D-BS-RK11-C-15 for the RKWC, RKBA, and their associated logic.

The RKWC performs a bus transfer word count operation. Initially, the register is loaded with the 2's complement of the number of words to be transferred to or from memory in the particular RK11 operation to be performed. Whenever 0 → NPR is generated, indicating a data word transfer complete, the RKWC is incremented. Also, the RKWC can be incremented by FAKE INC WC. FAKE INC WC is generated only for a Read Check (RD CHK) operation, because no data is transferred during a Read Check, therefore, 0 → NPR is not generated for each word transfer. However, data words are being transferred between the disk and RK11 Control and a word count must be maintained to define the number of words to be Read Checked. FAKE INC WC is generated in the RKDB control logic when data is enabled to transfer from the DSB to the RKDB during a Read Check operation only. When the value of the RKWC is 0, the register has essentially overflowed and 1 → WC OVF is generated which direct-sets the WC OVF flip-flop. Setting WC OVF inhibits further transfer and completes the previous data block transfer in the RK11.

The RKWC is loaded through the data lines of the bus. The RKWC value is loaded into the register by BUS → RKWC HI, BUS → RKWC LO, and LOAD REG. The bus gating signals are generated by the register selection logic, as well as LOAD REG. LOAD REG initiates the loading of RKWC in that it is keyed by the start of the transfer timing in the register selection logic.

The RKBA contains the address that specifies the memory location to or from which data is to be transferred to or from the RK11. The RKBA is incremented by two after each bus transfer; thus, the register continually points to sequential memory locations. The RKBA is loaded with the initial address from the bus data lines. This address is loaded into the register by BUS → RKBA LO, BUS → RKBA HI, and LOAD REG, which are generated in the register selection as the RKWC register loading signals. The RKBA incrementing by two is done by the assertion of 0 → NPR, which is generated in the NPR logic at the end of each data word transfer to or from memory. Therefore, the RKBA is incremented by two each time the RK11 performs an NPR. Unlike the RKWC, the RKBA is not needed for a Read Check operation, because no data is transferred into or out of the RK11 and, therefore, no bus address is required.

Each address that appears in the RKBA is available to the bus data lines (through the internal bus) and bus address lines for program use by addressing the RKBA. Bits 04 and 05 in the RKCS (EX0 and EX1) provide two added (most significant) bits to the RKBA. These bits provide for an increase of core memory locations above those that can be addressed in the RKBA. These bits are enabled by RKBA=ALL 1, which is generated when the RKBA overflows; this causes the extended RKBA bits to increment due to bus transfers. Bits 04 and 05 are loaded initially by the bus data lines (see engineering drawing D-BS-RK11-C-19). Care should be taken in making sure how much memory is available. When the RKBA contains any address that does not exist physically, NXM (nonexistent memory) will set in the RKER causing a hard error condition and terminating RK11 operation.

3.3 RK11 NON-TRANSFER FUNCTION LOGIC

The following paragraphs discuss the RK11 functions that do not perform a data transfer. These functions are: Control Reset, Drive Reset, Write Lock, and Seek functions. The Seek function is especially important in that it is used as part of the data transfer functions as well as alone. Also, the logic directly related to each of the RK11 non-transfer functions is discussed in the sequence in which each function is performed.

3.3.1 Seek Logic

The Seek operation positions the heads of the drive over the cylinder specified by the RKDA. This operation is initiated by loading the cylinder address into the RKDA off the bus D lines, by loading the function register for a Seek function (octal code 4), and by setting the GO bit in the RKCS.

Asserting GO generates T2 in the basic timing logic which, in turn, generates NEW FUNCTION. T2 also loads the INT FUN (internal function register) which is decoded to generate the SEEK signal in the major state logic. Asserting NEW FUNCTION generates the clocking signal 1 → MOVE HEADS in the Drive Read, Write, and Seek Control logic (see engineering drawing D-BS-RK11-C-07). The trailing edge of this pulse clocks the MOVE HEADS flip-flop, if DR PWR LO (drive power low) is unasserted indicating that the drive is operating in its optimum power range and if DRIVE OK is asserted, indicating that the drive is ready (DRY bit of the RKDS is set) and the heads are not moving (R/W/S RDY is asserted off the drive). The previous generation of SEEK sets the MOVE HEADS flip-flop when the clock is asserted.

Setting the MOVE HEADS flip-flop provides a gating signal with the cylinder address portion of RKDA to the drive address logic. MOVE HEADS gates each bit of the cylinder address to the cable drivers and generates

DR BUS STROBE, which gates the address into the address register of the drive logic. When the address is properly loaded into the drive address register, the drive responds with ADD ACK (address acknowledge) to the RK11 Control. ADD ACK clears the MOVE HEADS flip-flop which disengages the RK11 from the SEEK operation being performed in the drive. Asserting ADD ACK also generates SEEK STARTED in the polling logic which, in turn, generates 1 → XFC in the interrupt control logic. 1 → XFC sets the CONTROL READY bit in the RKCS. The RK11 is now ready for the next function. When the drive has initiated the Seek function, it asserts R/W/S RDY which, when MOVE HEADS is clear, generates INT ACC RDY (internal access ready).

In the case of a multiple-disk drive system, overlapping Seek functions can be performed. As soon as ADD ACK is asserted and SEEK STARTED sets ready, another Seek operation can be initiated to another drive etc., up to the total number of drives in the system. When overlapping Seek functions are performed, the RK11 has to be informed as to what drives have completed their Seek functions and the order of their completion. The hardware poling logic does this by polling each drive for Seek completions. It is here that the value of the Seek function becomes important. Write, WT CHK, Read, and RD CHK operations all perform their own Seeks to locate the desired cylinders on a disk. Therefore, for a single-drive system, Seek is a relatively redundant operation. However, in a multiple-disk system, due to the variable lengths of time the drives take to complete a Seek, overlapping Seek functions are a valuable tool. Initiating overlapping Seek functions can set up the drives for data transfer functions that can be performed as each drive reaches the desired cylinder. Because the present head position and the desired head position determine the time it takes for a Seek function to occur, polling allows the drives to be operated upon by the control as fast as each Seek is completed. This eliminates waiting for a drive to reach its addressed cylinder while another drive that is to be operated upon can reach its location sooner. The following paragraphs describe the polling process and its logic.

3.3.2 Hardware Poll Logic

The hardware poll allows the RK11 to have any or all drives performing a Seek or Drive Reset operation at a particular time. The RK11 hardware poll feature identifies the logical drive number, in the DRIVE ID bits of the RKDS, of any drive that has completed a Seek or Drive Reset function. The hardware poll feature will cause an interrupt provided: IDE in the RKCS is set, the READY bit in the RKCS is set, and the control is not already attempting an interrupt as a result of some other operation. This will occur even if IDE was not set when first initiating the Seek or Drive Reset function. If two or more drives complete the function simultaneously, the RK11 interrupts once for each drive and identifies each drive, in turn, in bits 13 through 15, RKDS. Ensure that the processor interrupt status flag is not raised to a level greater than or equal to that currently held by the RK11; otherwise, a second interrupt will occur immediately after the first and the end result will be the interruption of the interrupt service routine. This situation will also occur if a Seek operation is initiated to an address where the drive is located. The first interrupt will occur as a result of the successful initiation of Seek or Drive Reset. The second interrupt, which reports that the heads have reached their destination, will occur immediately, since the heads are at their destination.

Initiating the hardware poll is accomplished by asserting the POLL signals. These signals are asserted if: there are no hard errors (HE is clear); the RK11 is in the Idle major state; the register selection logic has not generated GATE RKDS → BUS; INT XFC is unasserted, which means the RK11 is not doing a data transfer operation; POLL DONE is unasserted: and CONTROL READY in the RKCS is set. (Refer to engineering drawing D-BS-RK11-C-12, Sheets 1 and 2, for the hardware poll logic.) Asserting the POLL signals enables the hardware poll clocking logic which generates a 4-μs delayed TEST POLL signal and a 100-ns clocking pulse train 1 → DR CNT (drive count), which clocks the drive count logic.

When a Seek function is initiated in a drive, the ADD ACK off the drive generates SEEK STARTED. This signal combines with disk select signal (SEL DSK 0 through SEL DSK 7), reflecting the particular disk selected to perform the SEEK, to generate the corresponding MASK bit. A MASK bit is set for each overlapping Seek performed on each disk. Therefore, the hardware poll can generate up to eight MASK bits (MASK 0 through MASK 7). Meanwhile, there are three DR CNT flip-flops that sequentially count (DR CNT 0 through DR CNT 2) from 0 to 7, for each 1 → DR CNT pulse that is generated by the hardware poll clocking logic. When the RK11 is polling (POLL asserted) the DR CNT states are gated into the disk selection logic and generate the DSK SEL signals that correspond to the disk designated by the DR CNT flip-flop states. When SEL MASK is asserted, POLL is asserted, and the disk designated by the SEL DSK signal asserts R/W/S RDY, INT SCH CMP (internal search complete) is set. However, if R/W/S RDY is not asserted, SIN (search incomplete) is generated by the drive which, combined with POLL, sets the SIN FLAG flip-flop. Setting SIN FLAG sets the SIN bit in the RKDS and the DRE bit of the RKER. When either of these flip-flops are set, the signal POLL DONE is generated. This signal disables the POLL signals which, in turn, stop the hardware poll clocking logic. If SCH CMP causes POLL to terminate, it is reflected by the fact that SCH CMP causes an interrupt request through the interrupt logic. If the interrupt is granted, RK INT MASTER is generated which, combined with POLL DONE, generates POLL INT DONE (poll interrupt done). This signal clocks the contents of the DR CNT flip-flops to the ID flip-flops (ID 0 through ID 2), which designate the DRIVE ID bits that caused the interrupt. Also, POLL INT DONE generates one more clock pulse to the DR CNT bits to put the count at the next disk code and initiate the LATCH decoder for the disk that caused the interrupt, which unasserts the respective LATCH signal for that disk. The LATCH signal clears the respective MASK bit, indicating that the POLL of the respective disk is complete. Finally, POLL INT DONE, if SIN FLAG is not set, generates 1 → SCH CMP, which sets SCP in the RKCS and informs the software that the previous interrupt was caused by a Seek function.

When the interrupt is granted, the software goes to a service routine that enables the operation to be performed on the disk that was polled. This occurs for each disk that performs a Seek until all the MASK signals are unasserted in the hardware poll logic.

3.3.3 Drive Reset Logic

The Drive Reset functions, specified by the octal code of six in the function register, are actually Seek functions to cylinder address zero of the disk. Like the Seek function, Drive Reset can be initiated on from one to seven disks, per one RK11, in an overlapping manner and use hardware poll logic. Drive Reset sets MOVE HEADS by generating NEW FUNCTION in the same manner as a Seek function, only that Drive Reset enables the data input to the MOVE HEADS flip-flop. However, generating DRIVE RESET asserts DRIVE RESTORE onto the disk drive cable, whereupon the drive logic directs the head movement to cylinder zero. Like a Seek function, the amount of time necessary to complete the function depends on the physical position of the heads at the time of initiation. The difference is that where a Seek function varies its head motion speed according to the distance the heads must travel, the Drive Reset function moves the heads at a constant speed. This is because in clearing the drive address logic for moving the heads to address zero, the drive no longer knows how far the heads have moved. Therefore, a constant speed is used to prevent the heads from crashing because they reached address zero without being able to slow down. A maximum Drive Reset, therefore, can take up to two seconds to complete.

3.3.4 Control Reset Logic

The Control Reset function, represented by a code of 0 in the RKCS function register, resets all RK11 register bits except RDY of the RKCS, which it sets, and bits 00 through 11 of the RKDS, which are unaffected. Control Reset also initializes all internal registers and flip-flops by generating the signal CONTROL CLEAR when T2 goes

low from the setting of GO in the RKCS (see engineering drawing D-BS-RK11-C-02). CONTROL CLEAR generates the signal INIT which is also generated by BUS INIT when the RK11 is initialized. Any effect of this function on a disk drive would occur as a result of clearing the RK11 controlling logic. This function is an effective *abort* because it stops all RK11 actions. Care should be taken in the use of Control Reset, however; if a Write function is in progress when the *abort* is issued, the remainder of that sector is destroyed and, therefore, the entire sector must be rewritten before any attempt can be made to read the sector. If Control Reset is used to abort a function currently in progress, so that a high-priority user may use the drive, the disk must first be checked for head motion before any new function can be initiated. This is indicated by RDY of the RKDS which reflects drive head motion. If the Check is not done, a hard-error condition can result and a Drive Reset function will have to be performed on that particular drive before it can be used again.

3.3.5 Write Lock Logic

The Write Lock function is loaded into the RKCS function register as an octal code of seven and initiates the generation of NEW FUNCTION. NEW FUNCTION combines with WRITE LOCK, which is generated by the function register logic, to assert WT PROTECT on the cable to the disk drive. Therefore, the WRITE LOCK function will write protect a selected drive until the condition is overridden by subsequent operation of the WT PROT switch on the corresponding drive control panel. The WRITE PROTECT status of a drive is reflected in the WPS bit of the RKDS. If a Write is attempted on a write protected drive the WLO bit of the RKER will set. This is a hard-error condition.

3.4 RK11 TRANSFER LOGIC

The following paragraphs discuss data transfer logic and data transfer-related logic. Also, the logic directly related to each of the RK11 functions is discussed by describing the sequence of logic steps when each of the functions is performed.

3.4.1 Major States (MSR) and Control Logic

While performing a data transfer function the RK11 goes through a sequence of six major states that describe the particular control function in relation to the data on the disk. A 6-bit major state register (MSR) counts the major states during which control and data transfer operations are performed. The six MSRs are: Idle, Preamble Header, Data. Checksum, and Postamble. (Refer to engineering drawing D-BS-RK11-C-04.)

In the Idle major state, the RK11 performs only non-data transfer functions or no function at all. Since the other major states reflect format areas of disk data information, non-data transfer functions can never be performed in these major states. Therefore, the Idle major state indicates that all data transfer paths are idle. The exception is the Read Check function. This function, by definition, is a non-data transfer function because it does not transfer data between the RK11 and the Unibus. However, the function does transfer data from the disk drive to the RK11. In this case, the function is utilizing and reading the disk formatted data and, therefore, will move through the logic major states. This is seen for the Read Check function as well as all the data transfer functions in the way the MSR shifts out of the Idle major state.

Control of the MSR is achieved by generating the CLR MSR and COUNT MSR signals (see engineering drawing D-BS-RK11-C-05). Each time COUNT MSR is generated, the MSR shifts to the next sequential major state. Therefore, for the MSR to move out of the Idle major state, COUNT MSR must be generated. From the Idle major state the setting of either the WRITE GATE or the READ GATE flip-flop will generate COUNT MSR. These flip-flops will set only if the RK11 is performing one of the three data transfer functions (Write Check, Write, or Read) or if the RK11 is performing a Read Check function. The actual conditions that set these flip-flops depend on the function that is being performed by the RK11. These conditions are described in subsequent paragraphs of this section in the discussions of each MSR-related function.

Generating CLR MSR clears the MSR back to the Idle major state. This signal is generated by GEN CLR, NEW SECT (see Paragraph 3.2.8), or by 0 → MSR. 0 → MSR is asserted for different conditions, depending on which MSR-related function the RK11 is performing. For a Read or Write function, 0 → MSR is generated when the last bit of the Postamble major state is reached. The last bit of the Postamble major state is determined in the Internal Word Count logic discussed in Paragraph 3.2.9. In the R/W A mode of operation, 0 → MSR is generated when WC OVF and LAST BIT are set. For any function, 0 → MSR is generated when a hard error condition occurs or when DRE is set, indicating that a drive error has occurred. Finally, 0 → MSR is generated during a Write or Write Check function (RD HEADER is set) when the header word off the disk is being checked in the Adder logic (CHECK HEADER is asserted).

The actual generation of each COUNT MSR and 0 → MSR in context of the MSR functions is described in the respective function discussions of this section. As previously stated, only Write, Write Check, Read, and Read Check functions sequence through the MSR states. All other functions are performed with the RK11 in the Idle major state.

3.4.2 Adder and Adder Control Logic

The Adder logic is enabled for one of two cases. That is, for any data transfer function, the Adder logic checks the header and the checksum. This Adder logic is enabled by MSR, RKDB, and RKDA. The ADDER CONTROL #1 flip-flop enables the header checking logic, and the ADDER CONTROL #2 flip-flop enables the Checksum Adder logic (see engineering drawing D-BS-RK11-C-14). The clocking signal (CLK ADDERS) clocks these flip-flops and the Adder network itself (see engineering drawing D-BS-RK11-C-15). CLK ADDERS is generated when either DSB → RKDB or LOAD RKDB is generated for a Read operation, or GATE BUS → RKDS is generated for a Write operation. Read Check and Write Check likewise generate these signals.

For a header check, ADDER CONTROL #1 (see engineering drawing D-BS-RK11-C-14) is direct set when the MSR is in the Header major state at LAST BIT (BC=17 * CLK LE), the RK11 is not in a Format mode operation, and the signal DSB → RKDB EN is asserted. DSB → RKDB EN is asserted by Read, RD CHK, or RD HEADER to include all conditions or functions, whereupon the Header will be checked. Setting ADDER CONTROL #1 generates CHOCS (check header or checksum) which drives a 1-μs one-shot. This output asserts CHECK HEADER if the MSR is not in the Postamble major state. Setting ADDER CONTROL #1 also generates the Adder gating signals RKDA → ADD; CHOCS H generates the gating signal $\overline{\text{RKDB}}$ → ADD. When neither Adder control flip-flop is set, CHOCS L is the asserted signal and RKDB → ADD is the asserted signal. Asserting these gating signals initiates the Adder for a header check by gating in the respective registers to the Adder network, which adds the corresponding bits of the RKDA with the complement of the RKDB. If the contents of the RKDA and RKDB are the same, indicating a correct header, the Adder (see engineering drawing D-BS-RK11-C-15) outputs zeros as it overflows. This condition is checked by gating all the Adder bit-by-bit outputs. If all the bits are zero, EQUAL is generated and the Header is correct. If the header addition shows that the added headers where not equal, then the input (EQUAL) is asserted to the SKE (SEEK Error) bit of the RKER, which is clocked by CHECK HEADER. This is a hard-error condition and will cause an interrupt to the processor.

Once the header has been checked, the ADDER CONTROL #1 flip-flop is unasserted and CHOCS goes low. MSR is now in the Data major state and the gating signals for the Adder being generated are now DATA → ADD and RKDB → ADD. These signals gate the previous value of the Adder and each sequential data word off the RKDB bit-by-bit for addition. This is done for each word transferred as each gating signal between the DSB and RKDB generates CLK ADDERS. When the transfer for the sector is complete, the Adder (see engineering drawing D-BS-RK11-C-15) contains the 16-bit sum of the data. This is the sector Checksum. When performing a Write operation, this value is gated to the RKDB to be written on the disk. However, if this is a Read, Read Check, or Write Check operation the value of the checksum in the Adder is checked against the checksum value coming off the disk into the RKDB.

When the checksum is checked, the last bit of the checksum (indicated by BC=17 * CLK LE), the MSR being in the Checksum major state, the DSB → RKDB EN gating signal, and FORMAT unasserted sets the ADDER CONTROL #2 flip-flop (see engineering drawing D-BS-RK11-C-14). Setting this flip-flop again generates CHOCS, which inhibits further checksum addition by removing RKDB → ADD and asserting $\overline{\text{RKDB}}$ → ADD. When the MSR enters the Postamble major state, which is automatic after the last bit of the checksum is in the RKDB, and the CSE (checksum error) of the RKER is clear, CHECK CHKSUM is generated. The gating signals that are now present cause the addition of the present checksum value calculated by the Adder and the complement of the checksum value located in the RKDB. If all the ADD bits output a zero, the checksum is correct and EQUAL is generated. If this is not the case, unasserting EQUAL will set the CSE bit of the RKER. This is a soft-error condition.

3.4.3 Disk Serial Buffer (DSB) Logic

The DSB is essentially a shift register that shifts data onto a disk for a Write function and serially assembles disk data for a Read function (see engineering drawing D-BS-RK11-C-06). The DSB is gated, in parallel, with the RKDB from where it loads data for serial transfer to the disk for a Write function or, after assembling a word, gates the word, in parallel, to the RKDB for a Read function. The DSB operates as if it were performing a Read when performing a Read Check, Write Check, and when reading a header during a Write function. Also, for a Write Check function, the DSB performs serial shifting as if performing a Write function. These functions are discussed in detail in the following paragraphs.

The DSB normally has the signal SHIFT EN asserted. The signal LOAD EN is asserted when SHIFT EN is unasserted. The conditions that disable SHIFT EN and enable LOAD EN, when performing a Write Check, are RD HEADER clear and SYNC BIT FOUND asserted. These conditions indicate that the sync bit of the Header coming off the disk drive has shifted into the DSB. The RKDB word can now be loaded into the DSB for the WT CHK comparison. During a Write function, END OF SYNC also causes LOAD EN to assert. LOAD EN asserted tells the RK11 that the sync area has been written and the header area is ready to be re-written onto the disk. LOAD EN loads this header value into the DSB for serial shifting to the disk. Finally, the last condition that generates LOAD EN is when LAST BIT is asserted in either the Header or Data major states for a Write or Write Check function when RD HEADER is off. This condition gates the contents of the RKDB to the DSB as each header or data word is ready to be gated to the DSB for serial shifting to the disk for a Write or for performing Write Check in the DSB. The SERIAL READ DATA flip-flop (see engineering drawing D-BS-RK11-C-07) contains each data bit being read for each CLK LE and inputs the DSB with the Read data. This data is shifted through the DSB until the data word is completely assembled, whereupon the RKDB initiates the gating signal for loading the word into the RKDB. SHIFT EN shifts each bit through from the SERIAL READ DATA flip-flop. For writing, LOAD EN and CLK TE generate RKDB → DSB which gates the contents of the RKDB into the DSB at the next CLK LE. Once loaded, the word is then shifted through the DSB (SHIFT EN asserted) and through the WRITE DATA flip-flop bit-by-bit and clocked by CLK LE to the disk. GEN DATA enables the DSB inputting as it reflects that MSR is either in header, data or checksum, which are all valid areas to be written. The way in which WRITE DATA sends the data to the disk is described in the Write logic discussion in the area of the DISK DATA flip-flop.

3.4.4 RKDB, Data Paths and Control Logic

The RKDB data paths are the gating circuitry that loads the RKDB with the contents of the data lines off the bus, the contents of the DSB, the outputs of the Adders, or the contents of the RKDA. What is loaded into the RKDB is determined by the gating signals generated in the RKDB Control logic. This logic generates the respective gating signals to the data path logic for loading of bus, DSB, Adder, or RKDA information. (The data path logic is shown on engineering drawing D-BS-RK11-C-21.) The RKDB control logic generates one of four gating signals to load the RKDB, depending on what has to be loaded as dictated by the logic that generates the gating signals (see engineering drawing D-BS-RK11-C-10). These gating signals are GATE BUS → RKDB, GATE DSB → RKDB, GATE ADDERS → RKDB, and GATE RKDA → RKDB.

GATE BUS → RKDB is generated during all data transfer operations except Read, only when NPR is set in the NPR logic. This gating signal, which loads the contents of the Unibus into the RKDB, is enabled by LOAD RKDB. LOAD RKDB is generated by the low transition of one of four ORed signal conditions. They are: GATE DSB → RKDB, ADDERS → RKDB SEQ, RKDA → RKDB SEQ, or DATA STR 1. GATE DSB → RKDB is generated for a Read, a Read Check, or when reading the header when LAST BIT is set and GEN DATA is asserted. GEN DATA is asserted when the MSR is in either the Header, Data, or Checksum major state. These conditions generate GATE DSB → RKDB with the presence of CLK TE. ADDERS → RKDB SEQ is generated for a Write or Write Check operation with R/W A cleared, the last word of the sector or data block in progress, and RKDB → DSB asserted. RKDB → DSB is asserted for a Write or Write Check operation when the data is loaded from the RKDB to DSB in the DSB logic. RKDA → RKDB SEQ is generated for a Write or Write Check operation, with R/W A clear and RD HEADER clear when the RK11 is in the Idle major state and COUNT MSR is asserted. This condition says that the header word to be re-written is in the RKDA and ready to move to the disk. Finally, DATA STR 1 is generated in the NPR logic for a Write function when the NPR has been initiated. This condition says that the RK11 has control of the bus for a Write function and is ready to load the RKDB with bus data.

GATE ADDERS → RKDB is generated for a Write or Write Check operation, with R/W A clear and LAST WORD IN PROGRESS asserted when LOAD RKDB is asserted. This condition says that the entire sector or data block is in the last word of a Write or Write Check and that the checksum is now calculated in the Adder. GATE ADDERS → RKDB loads the checksum into the RKDB to be written on the disk or to be Write Checked with the data block already on the disk.

GATE RKDA → RKDB for a Write or Write Check with R/W A and RD HEADER clear when LOAD RKDB is asserted and the RK11 is in the Preamble major state. This gating signal indicates that the RK11 is about to enter the Header major state where it re-writes the header on the disk. This header value is obtained from the RKDA and must be loaded into the RKDB by the Header major state to be written on the disk correctly.

The signals 1 → RKDB 00 through 1 → RKDB 15 output by the data paths are the inputs of the RKDB (see engineering drawing D-BS-RK11-C-11). The generation of any of these data path outputs sets the respective bit of the RKDB.

3.4.5 Write Logic

The Write operation consists of performing a Seek to the cylinder address on the disk specified in the RKDA, reading and checking the header, finding the sector designated in the RKDA on the disk, loading the HEADER for re-writing on the disk, re-writing the header on the disk, loading the data off the bus and writing it on the disk, calculating and writing the checksum, and terminating the Write function. These Write function steps are directed by the MSR and MSR control logic. The MSR major states are directed and controlled by the RD GATE, WT GATE, and the bit counter and internal word count logic. The clocking and transfer of data to the disk is generated on engineering drawing D-BS-RK11-C-07 along with the MOVE HEADS, RD GATE, WT GATE, and SC=SA logic. Throughout the discussion of the Write function the logic being discussed is referenced by name to sections previously described and/or by referencing the respective engineering drawings that contain the logic being discussed.

The initiation of all data transfer functions begins with an implied Seek function. That is, the RK11 directs the addressed drive to move its heads to the cylinder address specified in the cylinder address portion of the RKDA

by setting MOVE HEADS, which also clears the MSR to IDLE. As explained in the Seek logic discussion, the drive address logic has accepted the address and is directing its heads to the address by returning ADD ACK to the RK11. When the drive sets the R/W/S RDY bit of the RKDS, which says the drive heads are over the specified cylinder address, INT ACC RDY is generated. At this point, the drive is positioned over the proper cylinder and is ready to check the header.

When MOVE HEADS was set at the initiation of the implied Seek, the fact that the RK11 was performing a Write function also sets the RD HEADER flip-flop. Coming off the drive, INT ACC RDY generates XFER COND (see engineering drawing D-BS-RK11-C-07) which, along with RD HEADER set, sets the RD GATE flip-flop. In the MSR control logic, setting the RD GATE when the RK11 is in the Idle major state generates COUNT MSR, which shifts the MSR to the Preamble major state. In DSB logic, SHIFT EN is the normally asserted signal generated when the input conditions are unasserted. Therefore, when the drive heads pick up the sync bit of one of the cylinder headers, bit 15 of the DSB goes to one and SYNC BIT FOUND is generated in the MSR control which, in turn, asserts COUNT MSR. The MSR now shifts to the Header major state. The DSB was able to read the sync bit in that with the RD GATE set the appearance of STD RD DATA (standard read data) in the basic timing from the drive set the SERIAL READ flip-flop. The SERIAL READ DATA flip-flop inputs the DSB with data off the drive cable receivers. The DSB, now in the Header major state, assembles the header word from the drive. When the header word is complete, the LAST BIT flip-flop is set in the bit counter logic (see engineering drawing D-BS-RK11-C-09), meaning the counter has counted 17_8 bits (BC=17 * CLK LE). In the RKDB control logic (see engineering drawing D-BS-RK11-C-10) with RD HEADER set and GEN DATA asserted, as defined in the MSR control logic, LAST BIT generates GATE DSB → RKDB and the contents of the DSB are loaded into the RKDB. Previously in the RKDB control logic when RD HEADER set, DSB → RKDB EN was asserted. Now the setting of LAST BIT, along with the presence of DSB → RKDB EN, sets the ADDER CONTROL #1 flip-flop in the Adder logic. BC=17 * CLK LE reflects the LAST BIT condition and with the RK11 in the Header major state, the setting of ADDER CONTROL #1 flip-flops, in turn, generates CHECK HEADER. The generation of CHECK HEADER initiates the Adder logic to check the header. In the MSR logic, CHECK HEADER generates 0 → MSR which, in turn, clears the MSR and RD GATE. This puts the MSR back in the Idle major state. When EQUAL is generated in the Adder logic, due to a correct header check, the HEADER OK flip-flop is set (see engineering drawing D-BS-RK11-C-07). The setting of HEADER OK clears the RD HEADER flip-flop. The RK11 is ready to re-write the header and begin data transmission to the disk. First, however, the drive heads must be in position for the transfer at the correct disk sector in the cylinder chosen.

The sector counter portion of the RKDS contains the sector count or address of the present sector at the drive heads. The sector address portion of the RKDA contains the sector address of the sector on the disk designated to be operated on. This sector address in the RKDA is loaded by program control and is compared to the sector count of the RKDB through a comparison gating circuit (see engineering drawing D-BS-RK11-C-07). When the sector address in the RKDS equals that of the RKDA the signal SC=SA is generated. When HEADER OK is set, because of a correct Header check, SC=SA then sets the WT GATE flip-flop. WT GATE generates another COUNT MSR and the MSR shifts to the Preamble major state and begins writing the appropriate sync area on the disk. The control is now ready to load the header for re-writing on the disk.

In the Preamble major state, for a Write function, the RKDB control logic generates the gating signal GATE RKDA → RKDB, which gates bits 5 to 12 of the RKDA to the RKDB. At this point, the RK11 needs the assertion of END OF SYNC to move the Header major state. Since the initiation of the Write function and when the RK11 moves out of the Idle major state, the bit counter and internal word count logic have counted for each CLK LE pulse. This CLK LE pulse is initiated by setting WT CLK and pulse for each bit time (see engineering drawing D-BS-RK11-C-02). When SYNC OVF is generated at the specified internal word count (see Paragraph 3.2.9), the Preamble has been counted and the disk is ready for the header. SYNC OVF at BC=17 * CLK LE, with PREAMBLE and WT GATE asserted, sets the END OF SYNC flip-flop in the MSR control logic. This causes another COUNT MSR; the MSR now shifts to the Header major state. END OF SYNC generates LOAD EN in the DSB logic which loads the contents of the RKDB into the DSB. END OF SYNC also sets the WRITE DATA flip-flop which, with WT GATE set, writes the sync bit (see engineering drawing D-BS-RK11-C-07). The RK11 is now ready to write the header on the disk and begin loading data off the bus, loading it into the DSB, and serially writing it on the disk.

The write clocking logic provides the WT CLK signal from a M405 crystal oscillator to the RK11 logic. Also, the clocking logic clocks the data from the WRITE DATA flip-flop of the DSB logic to the write logic of the disk drive. Figure 3-1 is the timing diagram for the write clocking logic. This logic is driven by a crystal oscillator that enables the clock input of the H/L (high/low) flip-flop when the WT GATE is set. H/L adjusts the clock signals for either a high- or low-density disk. For a high-density disk, H/L is driven and held high until the flip-flop is cleared (GEN CLR + NEW SECT). For a low-density disk, the input LO DEN is asserted (reflects the state of bit 11 of the RKDS) and each clock input causes H/L to toggle. Therefore, the H/L flip-flop is held high for every other clock input. When H/L is high and WT GATE is set, the clock input to the DIV 2 flip-flop is asserted. This also causes a toggle action that generates one pulse for every two clock inputs. DIV 4 repeats this toggle action keying on the DIV 2 outputs and DIV 4 outputs for every two DIV 2 inputs. Therefore, DIV 2 divides the input clock by two, and DIV 4 divides the DIV 2 signal by two again. DIV 2 inputs the WT CLK flip-flop which generates the clock output to the basic timing logic to generate CLK LE and CLK TE. Each time the DIV 4 flip-flop goes low the next clock toggles the DISK DATA flip-flop. This condition defines the bit area being sent to the drive. When WRITE DATA is asserted, reflecting a 1 bit being written, DIV 4 high toggles DISK DATA at the next clock. This condition puts an output pulse between the pulses that defined the bit area; the drive write logic recognizes the bit as a one. WRITE DATA is asserted every time SHIFT EN in the DSB logic shifts a one to WRITE DATA. Therefore, the header is written and clocked to the disk drive. The RK11 is now ready to load the RKDB with bus data and write it on the disk.

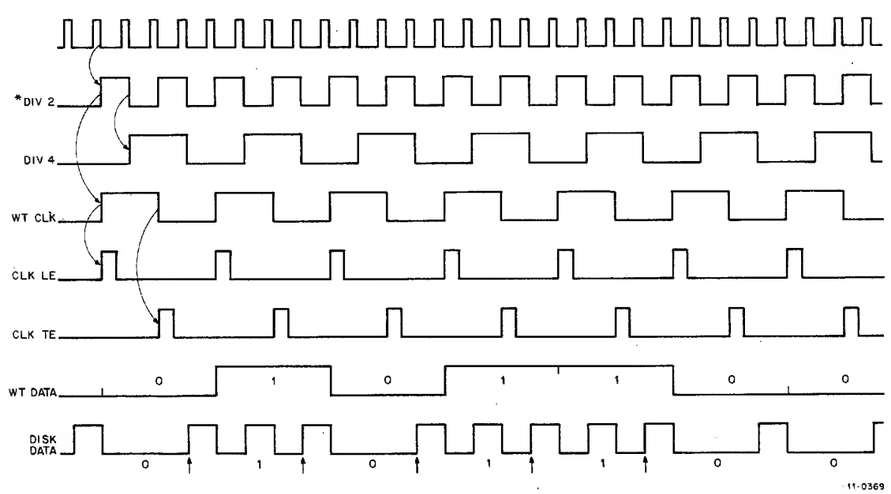


Figure 3-1 Write Clocking Logic Timing Diagram

In RKDB logic (see Paragraph 3.4.4), an NPR for each word through the NPR flip-flop and the NPR logic generation of DATA STR 1 for a Write, generates GATE BUS → RKDB. This signal loads the data word off the bus and into the RKDB. Each time LAST BIT is set in the bit counter logic, during a Write when RD HEADER is off and the RK11 is in either the Header or Data major state, the DSB logic asserts LOAD EN which loads the newly assembled word, off the bus, from the RKDB to the DSB where it is immediately shifted through the write clocking logic to the disk write logic by SHIFT EN. When LAST BIT was set by the writing of the HEADER, MSR shifted to the Data major state whereupon the DSB loading/shifting process continues, but now gating the data off the bus. When LAST WORD DONE is set in the counter logic (see engineering drawing D-BS-RK11-C-09) by reaching the end of a sector, the MSR control causes the MSR to shift to the Checksum major state. The RK11 is now ready to load the calculated Checksum into the RKDB from the Adders and send it to the drive write logic.

In the RKDB control logic, LAST WORD IN PROGRESS generates GATE ADDERS to RKDB. The RKDB is loaded with the Checksum value calculated in the Adder logic. The Checksum is sent to the DSB and out through the write clocking logic the same as a data word. When LAST BIT again sets the MSR shifts to the Postamble major state. At this point the RK11 will stop or continue, depending on the word count (RKWC).

For the Write function in the Postamble major state an internal word count of 4 (IWC 2 set) permits the writing of 4 words of Postamble. At IWC 2 when LAST BIT is set, 0 → MSR is generated in the MSR control logic and MSR clears to the Idle major state. If the Write function is to continue into a new sector, the Write function starts again by re-writing the header. This re-start for a new sector under the same block data transfer is initiated by NEW SECT in the basic timing logic. This will occur as long as RKWC has not overflowed signaling the end of the data block to be transferred. When WC OVF appears further transfers are inhibited through inhibiting further NPRs. If this occurs in the middle of a sector, data transfer stops, but the RK11 continues to sequence to the end of the sector and still writes the checksum. When a Write function continues to the next cylinder, COUNT DA and RKDA 04 in the RKDA logic re-initiate the entire Write function by setting MOVE HEADS and RD HEADER. COUNT DA increments the cylinder address and the header value is at the next cylinder address in the RKDA to correspond to the new value being read off the disk. Trying to continue writing beyond the last cylinder on the disk cannot be done and will cause an OVERRUN error, which is a hard error.

3.4.6 Read Logic

The Read function consists of performing an implied Seek to the correct cylinder address on the disk, finding the designated sector on the disk, reading the header and checking it, reading data off the disk and transferring it to the bus, calculating the checksum and checking it with the value being read off the disk, and terminating the Read function. These Read function steps are directed by the MSR and MSR control logic. The MSR control is directed by the internal word count and bit counter logic (see engineering drawing D-BS-RK11-C-09). The Read function clocking and timing is generated in the Read logic of the disk and asserted in the RK11 basic timing logic. Throughout the discussion of the Read function the logic discussed is referenced either by the name by which it has been described previously in the chapter or by referencing the respective engineering drawings whose logic is being described.

The initiation of the program-controlled Read function begins with an implied Seek function. This operates the same as that for a Write with the setting of MOVE heads. INT ACC RDY signals the RK11 that the drive has performed the Seek function and can now begin reading the header. MOVE HEADS is now clear and, unlike the Write operation, the RD HEADER flip-flop is never set. INT ACC RDY has also generated XFER COND (see engineering drawing D-BS-RK11-C-07).

The drive heads are now positioned over the cylinder address specified in the drive address logic. At this point, for a Read function, the RK11 waits for the comparison gating circuit (see engineering drawing D-BS-RK11-C-07) to assert SC=SA which indicates that the designated sector is approaching the drive heads. SC=SA, along with the previous generation of XFER COND, sets the RD GATE flip-flop. As soon as the drive Read logic begins transmission of the Header to be followed by data to the RK11, STD RD DATA appears in the basic timing logic. STD RD DATA, along with the RD GATE flip-flop being set, sets the SERIAL READ DATA flip-flop. When the RD GATE flip-flop was set the RK11 shifted from the Idle major state to the Preamble major state, because the RD GATE generated COUNT MSR in the MSR control logic. At this point, the RK11 is ready to begin the Read data transfer operation.

The RK11 remains in the Preamble major state until SERIAL READ DATA is set. This, with SHIFT EN asserted in the DSB logic, sets DSB 15 with the header sync bit, which causes another COUNT MSR in the MSR control logic and the MSR shifts to the Header major state. The DSB then shifts in the entire header which, when completely assembled in the DSB, causes LAST BIT to set in the bit counter logic (see engineering drawing D-BS-RK11-C-09). In the RKDB control, setting LAST BIT generates GATE DSB → RKDB, when the RK11 is in the Header or Data major state (GEN DATA) for a Read function. Therefore, the header is now loaded into the RKDB. When the RK11 shifted to the Header major state at the setting of LAST BIT (BC=17 * CLK LE) the ADDER CONTROL #1 flip-flop was set in the Adder logic. This generates CHECK HEADER and the Header value read off the disk is checked with that of the RKDA. This occurs when the header is loaded into the RKDB as indicated to the Adder logic with the generation of CLK ADDERS. A correct header check sets the HEADER OK flip-flop (see engineering drawing D-BS-RK11-C-07). The setting of LAST BIT during the Header major state causes the RK11 to shift to the Data major state. The RK11 now begins to read data and must establish NPR for data transfer to the bus.

The generation of GATE DSB → RKDB for a Read function causes a clock to the NPR. If no error conditions exist, the NPR sets. Granting NPR generates NPR GATE RKDB → BUS in the NPR logic which, in turn, generates RKDB → BUS in the RKDB logic. This gates the contents of the RKDB to the internal bus which inputs the bus drivers and transfers the data onto the bus. Each time LAST BIT is set GATE DSB → RKDB is generated which, in turn, causes an NPR for each word. This occurs for every word until either RKWC overflows or the end of the sector is reached and the checksum is calculated.

When LAST WORD DONE is asserted by the internal word count logic (see engineering drawing D-BS-RK11-C-09) the MSR shifts to the Checksum major state. At BC=17 * CLK LE the ADDER CONTROL #2 flip-flop is set terminating the Adder operation. During the reading of data, the Adder logic has been adding each data word in its logic. The value present in the Adders at the Checksum major state is now the calculated checksum. Also, the the Checksum major state, the RK11 reads the checksum value off the disk and loads it into the RKDB; any NPR is inhibited. When LAST BIT appears in the Checksum major state, the MSR shifts to the Postamble major state. The Adder logic now generates CHECK CHECKSUM and the contents of the complemented RKDB are gated to the Adders and checked against the calculated checksum value. If the checksum did not compare the CSE (checksum error) bit of the RKER is set.

When LAST BIT sets during the Postamble major state, 0 → MSR is generated which, in turn, generates CLR MSR and the MSR clears to the Idle major state. This also clears RD GATE. If the Read function is to continue into a new sector, Read starts again with SC=SA. The generation of NEW SECT in the basic timing logic clears the RK11 flip-flops and the Read function will resume as long as RKWC does not overflow signaling the end of a block transfer. When WC OVF appears further transfers are inhibited by inhibiting further NPRs. If WC overflows in the middle of a sector, data transfer stops, but the RK11 continues to sequence to the end of the present sector and still checks the checksum. Like the Write function, the Read function can continue onto the next cylinder, except that RD HEADER never sets. A Read function cannot sequence to another disk drive without causing a hard error.

3.4.7 Read Check Logic

The Read Check function is identical to a normal Read function except that no NPRs occur. This means that the entire operation performs no data transfer to the bus. Data transfer is performed only between the drive and the RK11. The Read Check function is, in essence, a parity check; data is read off the disk and the checksum is calculated and checked in the RK11. Therefore, this function enables the program to know beforehand if a given record is readable and error free.

Initially, the RK11 performs the implied Seek for the Read Check and the drive Heads are aligned at the designated cylinder. When SC=SA the RD GATE flip-flop is set, shifting the MSR to the Preamble major state and setting SERIAL DATA READ when the drive transmits the data (SRD RD DATA). When the HEADER sync bit sets DSB 15 in the DSB logic, the MSR shifts to the Header major state and ADDER CONTROL #1 flip-flop is set in the Adder control logic. This enables CHECK HEADER and the Adder logic holds for the header to be shifted to the RKDB. When LAST BIT is set in the bit counter logic, GATE DSB → RKDB loads the DSB contents into the RKDB. The Adder logic now checks the header and, if correct, EQUAL sets the HEADER OK flip-flop (see engineering drawing D-BS-RK11-C-07). An error would abort operation through SKE of the RKER. Keying on LAST BIT the DSB reads the disk data as the MSR shifts to DATA which is loaded into the RKDB by GATE DSB → RKDB. The Adder logic calculates the checksum as each word enters the RKDB. Once in the Data major state, the RKDB control logic for a Read Check issues a FAKE INC WC (fake increment word count) for each word. This controls the amount of data to be read checked. Because a Read Check function performs no data transfers to the bus, RKWC is not incremented as it would be for a Bus Transfer function. However, the data block to be read checked must be defined and must generate WC OVF when finished. Therefore, FAKE INC WC is generated to keep track of the function. When LAST WORD DONE is asserted in the internal word count logic, the RK11 shifts to the Checksum major state and the disk checksum value is read and loaded into the RKDB. LAST BIT shifts the MSR to the Postamble major state and the Adder logic is initiated to check the checksum. Asserting EQUAL allows the function to terminate or move to the next sector. If EQUAL is not asserted, CSE is set in the RKER and the data is in error. The Read Check operation terminates in the same way a Read function terminates.

3.4.8 Write Check Logic

The Write Check function is used to compare, bit by bit, the contents of memory to the contents of a continuous block of data on a disk. These two areas, due to a previous Write function, contain identical data. The Write Check function compares the disk and memory to see if the previous Write function transferred the data correctly.

At the initiation of the Write Check function, the RK11 performs the implied Seek as it does for a Write function. In this case, RD HEADER is set as well as MOVE HEADS. RD HEADER sets the RD GATE flip-flop and the MSR shifts to the Preamble major state. The appearance of the sync bit at DSB 15 shifts the MSR to the Header major state and the header is assembled in the DSB. At this point the Adder logic is initiated and CHECK HEADER generates 0 → MSR in the MSR control logic to clear the MSR back to IDLE and reset RD GATE. Meanwhile, the Adder logic checks the header value read into the RKDB with that of the RKDA. For a correct header, EQUAL sets the HEADER OK flip-flop which clears the RD HEADER flip-flop. The RK11 now looks for SC=SA whereupon it will begin write checking the corresponding data blocks.

When SC=SA appears, RD GATE is set once more and the MSR shifts to Preamble. At this point the RKDB control logic generates GATE RKDA → RKDB which shifts the RKDA cylinder address portion to the RKDB. When DSB 15 is set, because of the sync bit coming from the disk, the DSB logic generates LOAD EN for the WT CHK and the RKDB value is loaded into the DSB. Also, SYNC BIT FOUND shifts the MSR to the Header major state. The DSB then resumes shifting with SHIFT EN. The DSB shifting now shifts the word from the disk through DSB 15 and shifts the loaded word from the RKDB out through the WRITE DATA flip-flop. At any time DSB 15 and WRITE DATA represent the corresponding bits of each word. These two bits are compared in the Error logic (see engineering drawing D-BS-RK11-C-16). An identical comparison means that the respective bits of each word are correct. An unfavorable comparison causes the WCE bit (write check error) to set in the RKER; this is a soft-error condition. When LAST BIT is set in the bit counter logic, the MSR shifts to the Data major state and the comparison continues; however, the data loaded from the RKDB must now be gated to the RKDB from the bus. This is done through the NPR for a Write Check function which generates GATE BUS → RKDB in the RKDB control logic, for each NPR and, therefore, for each word of data. When LAST BIT is set for each of the words shifting through the DSB during Write Check, LOAD EN is asserted each time. This loads each word into the DSB as the DSB finishes shifting the previous word of the Write Check. LAST WORD DONE shifts the MSR to the Checksum major state where the DSB begins to assemble the disk checksum value. Meanwhile, LAST WORD IN PROGRESS has generated GATE ADDERS → RKDB which gates the calculated checksum from the Adders to the RKDB. The LAST BIT assertion for the last bit of the last word of data, which causes the shift to Postamble, also asserts LOAD EN; the calculated checksum is loaded into the DSB as the RK11 enters the Checksum major state and begins reading the disk checksum. This is the last write check of the sector whereupon LAST BIT shifts the MSR to Postamble. The Write Check function now terminates in the same manner as a Read function. The Write Check function may be initiated with less than whole sector boundaries if the number of words to be write checked is exactly the same as the number of words written.

3.4.9 Read/Write All (R/W A) Mode Logic

The Read/Write All mode of operation for the RK11 is only performed in conjunction with a Read or Write operation. As with normal Read or Write functions, the RK11 in the R/W A mode performs the implied Seek function to the designated cylinder address after which it searches for SC=SA. As soon as SC=SA is asserted either the Read or Write logic of the RK11 and the drive are initiated. After every 16 bits a word is transferred to or from memory, respectively. The major difference in this mode is that there is no hardware check of head positioning (header check). Also, the RKDA does not increment until the end of a transfer. If the RKWC has not overflowed in one disk revolution the control will not go to the next surface or next cylinder. In the latter case, the R/W A function will just wrap around itself on the same cylinder surface until RKWC overflows.

This mode of operation simulates formats to be written or read on controllers other than the RK11s. To simulate another format, the programmer must thoroughly understand the alien format and carefully construct its sync area, all data, and any checking codes through the software. In line with this, it must be kept in mind that the RK11 reads and writes least significant bits first. An IBM 2315 type disk cartridge with any number of sectors up to 16_{10} may be used in this mode.

On engineering drawing D-BS-RK11-C-07 for a Write function in the R/W A mode, the appearance of SC=SA in the logic will set the WT GATE if R/W A is set (bit 9 of the RKCS). Therefore, in this mode the WT GATE is enabled without waiting for HEADER OK. In fact, the RD HEADER flip-flop is inhibited from setting by the On state of R/W A. In the MSR logic the termination of the major state logic, through 0 → MSR with R/W A set, is done with WC OVF which corresponds to this mode of operation. R/W A also inhibits the Adder and RKDA gating signals for a Write in the RKDB control logic.

3.4.10 Format Mode Logic

The Format mode of operation for the RK11 is only used in conjunction with normal Read or Write functions. This mode is used to format a new disk cartridge or to reformat any sector that may have been erased or damaged due to RK11 or drive failure.

In the Format mode, the Write function is performed in the same manner as that for normal operation except that the drive heads are not checked for proper position before writing begins. Under normal operation the RK11 rewrites the header in Write operation each time the associated sector is written. When FMT (format) is set in the RKCS under program control, the presence of SC=SA will set the WT GATE. Also, RD HEADER is inhibited and, therefore, a header check cannot take place.

In the Format mode, the Read operation is performed in the same manner as that for normal operation except only one word per sector, the header word, is transferred to memory. Therefore, a 3-word Read function in the Format mode will transfer three contiguous header words to three consecutive memory locations for software checking. This is due to the fact that an NPR is generated in the Format mode only when the RK11 is in the Header major state (see engineering drawing D-BS-RK11-C-11). Terminating a Read or Write in the Format mode is the same under normal operation.

3.5 ERROR DETECTION LOGIC

The RK11 error conditions are indicated in the RKER and by bits 14 and 15 of the RKCS. Each of the error condition bits is described and defined in Chapter 2. Bit 15 of the RKCS (ERR) is set when any of the RKER bits are set and bit 14 of the RKCS (HE) is set when any of bits 05 through 15 of the RKER are set. Bit 00 (WCE) and bit 01 (CSE) are soft error conditions of the RK11. They will only cause an interrupt when SSE (stop on soft error) of the RKCS is set with IDE (interrupt done enable) set in the RKCS. The other RKER error conditions are hard errors and will cause an interrupt when IDE is set. The logic for the RKER error conditions is shown on engineering drawing D-BS-RK11-C-16. The DRE (drive error) bit of the RKER reflects status information from the RKDS that indicates the drive is not ready for operation. The other error conditions reflect RK11 and bus transfer errors. The bit definitions contained in Chapter 2 and the engineering drawings fully describe the initiation of an error condition.

3.6 MAINTENANCE MODE LOGIC

RK11 maintenance mode operation is achieved by the programmed setting of M (bit 12) in the RKCS. Setting this bit inhibits any signals from being transmitted to or from any disk drive and permits diskless operation of the RK11. This bit is used in conjunction with the RKMR which is the maintenance register that simulates drive signals. These simulated signals are defined in the RKMR (see engineering drawing D-BS-RK11-C-15) discussion in Chapter 2. The RKMR, when M is set, simulates the sector count, R/W/S RDY, DRY, MLAI (simulates an NXD condition), MADA (simulates ADD ACK), sector pulse, read data pulse, and the read clock pulse. The RKMR is program-controlled and its specific operation is discussed in Chapter 6.

CHAPTER 4
MODULE DESCRIPTIONS

4.1 INTRODUCTION

This chapter describes special modules used in the RK11 Disk Control Unit, that is, certain modules that are not described in other PDP-11 documentation or those not described in the *DEC Logic Handbook.* Table 4-1 lists all the modules used in the RK11 System and references where these modules are described.

4.2 DEC LOGIC

The compatible above-ground DEC logic generally operates with levels of ground to +0.4V (lower level) and +2.4V to +3.6V (upper level), using TTL or TTL-compatible circuits with inputs that supply current at ground and outputs that sink current at ground. Figure 4-1 shows the TTL logic voltage spectrum.

The use of DEC's *Digital Logic Handbook,* 1970 edition, is recommended for readers of this manual who are not familiar with the basic principles of digital logic and the type of circuits used in DEC logic modules.

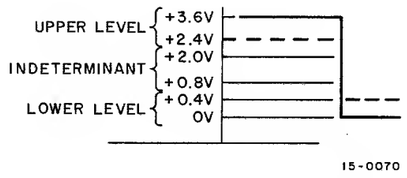


Figure 4-1 Voltage Spectrum of TTL Logic

4.3 MEASUREMENT DEFINITIONS

Timing is measured with the input driven by a gate or pulse amplifier of the series under test and with the output loaded with gates of the same series (unless otherwise specified). Percentages are assigned with 0 percent indicating the initial steady-state level and 100 percent indicating the final steady-state level, regardless of the direction of change.

Input/output delay is the time difference between input change and output change, measured from 50 percent input change to 50 percent output change. Rise and fall delays for the same module are usually specified separately.

Rise time and fall time are measured from 10 percent to 90 percent of waveform change, either rising or falling.

4.4 LOADING

Input loading and output driving for TTL logic are specified in "units", with one unit equivalent to 1.6 mA. The inputs to low-speed gates usually draw one unit of load. High-speed gates draw 1.25 low-speed units, or 2 mA.

4.5 MODULE CHARACTERISTICS

The following paragraphs describe the characteristics of the RK11 System's special modules. Also included are any special maintenance modules and the characteristics of the system's power supplies. The schematic and component location diagrams for the special modules are located in the *RK11 Disk Drive Control Engineering Drawings* volume that is supplied with the shipped system.

4.5.1 G736 Priority Select Module

The G736 is a single-height module used to interface PDP-11 devices to the interrupt structure of the Unibus. The module contains a 14-pin IC socket which is designed to take specially etched chips for selection of an interrupt level from BR4 to BR7. These chips allow the RK11 to discontinue the BR GRANT LINE to which the device is assigned.

4.5.2 G740 Disk Selection Module

The G740 is a single-height module used to jumper up to eight select lines to eight input signals. Split lugs are provided on the module for ease of inserting or removing jumpers. Each unjumpered output is clamped at +3V. Therefore, when a low or 0V is asserted at an input pin, the corresponding output to which it is jumpered is driven low.

The input pins are labeled from 0 through 7, while the output pins are labeled A through J, respectively.

4.5.3 M116 6 4-Input NOR Gate Module

The M116 is a single-height module which provides 4-input NOR gate functions for general applications. The M116 Module contains six of these 4-input NOR gates.

Inputs:	Each of the 24 inputs of the 6 gates represents 1 TTL load. Unused inputs must be returned to ground.
Outputs:	Capable of driving 16 TTL unit loads with a maximum of 13 ns propagation delay. Source of +3V available at pins U1 and V1.
Power:	Each input is driven by a nominal voltage of +5V with a ±0.25V tolerance and draws a current of 30 mA.

Table 4-1
Module Utilization

Module Number	Quantity Used	Title	Reference
G736	1	Priority Selection	3
G740	1	Disk Selection	3
M002	1	Logic 1 Source	1
M105	1	Address Selector	1,2
M111	2	Inverter	1
M112	5	NOR Gate	1
M113	7	10 2-Input NAND Gates	1
M115	3	8 3-Input NAND Gates	1
M116	3	6 4-Input NOR Gates	3
M117	3	6 4-Input NAND Gates	1
M119	2	3 8-Input NAND Gates	1
M121	3	AND/NOR Gates	1
M141	2	NAND/OR Gates	1
M149	10	9 x 2 NAND Wired OR Matrix	3
M161	1	Binary to Octal/Decimal Decoder	1
M163	1	Dual Binary to Octal Decoder	3
M203	4	8-R/S Flip-Flops	1
M205	3	5 "D" Flip-Flops	3
M207	1	J-K Flip-Flops	1
M208	2	8-Bit Buffer/Shift Register	1
M214	3	Adder Register	3
M216	5	Six Flip-Flops	3
M236	1	Binary Up/Down Counter	1
M238	1	Synchronous 4-Bit Up/Down Counter	3
M239	2	Three 4-Bit Counter Register	3
M304	3	One-Shot Delay – Pulse Amplifier	3
M307	3	Integrating One-Shot	3
M405	1	Crystal Clock 5.760 MHz	1
M611	1	Power Inverter	3
M617	1	4-Input Power NAND Gate	1
M623	3	Bus Driver	1
M782	1	Interrupt Control	1,2
M784	3	Unibus Receivers	1,2
M795	1	RKWC and RKBA	2
M796	1	Unibus Master Control	2
M797	1	Register Select	3
M798	1	Unibus Drivers	2
M930	1-3	Bus Terminator	1
H720 E(F)	1/System	Power Supply (RK11)	4
H734 A(B)	1-4/System (1/two disk drives)	Power Supply (RK02, 03, 04, or 05)	3

References:
1. *DEC Logic Handbook*
2. *PDP-11 Unibus Interface Manual* (DEC-11-HIAA-D)
3. Special Modules Covered in this Chapter
4. *H720 Power Supply and Mounting Box Manual* (DEC-11-HR5A-D)

4.5.4 M149 9 x 2 NAND Wired OR Matrix

The M149 is a single-height module containing two sets of 9 open collector NAND gates wired together in an OR function to form nine output pins. The M149 also includes a pulse amplifier.

Inputs: Voltages are standard TTL levels. Input loading is 1 unit per input.

Outputs: Voltages are standard TTL levels. Each output except V1 is an open collector that can sink 16 mA. The output at V1 can drive 10 unit loads.

Input/Output Delay: 10 ns at output

Power Dissipation: 350 mW

Application: This module is generally used to gate signals onto an open collector bus.

4.5.5 M163 Dual Binary-to-Decimal Decoder

The M163 consists of two independent binary-to-decimal decoding structures on a single-height module. Each decoder produces a negative true (0V) output for the decimal equivalent of the binary input.

Each decoder can also be used for octal or quad decoding by grounding the MSB, or MSB and the next MSB input lines. Each decoder has a propagation delay of 40 μs (maximum) for input-to-output turnon or turnoff.

Inputs: Voltage levels of 0V and +3V (typical). All inputs represent 1 TTL unit load each.

Outputs: Voltage levels of 0V and +3V (typical). All outputs are capable of driving 10 TTL unit loads.

Power: 58 mA (typical) at +5V.

4.5.6 M205 5 "D" Flip-Flops

The M205 module contains five separate D-type flip-flops. Each flip-flop has independent DATA, CLOCK, SET, and CLEAR inputs. Information must be present on the DATA input for 20 ns (maximum) before the CLOCK pulse; the information should remain at the input at least 5 ns (maximum) after the CLOCK pulse has passed the threshold voltage. Data transferred into the flip-flop by the previous CLOCK pulse will be present on the 1 output of the flip-flop. Typical time duration of the CLOCK pulse preset and reset pulses is 30 ns each. Maximum delay through the flip-flop is 50 ns. Refer to the M206 description for additional details.

The following are the input, output, and power characteristics of the M205 module.

Inputs: D inputs represent 1 unit load each.
C inputs represent 2 unit loads each.
SET inputs represent 2 unit loads each.
CLEAR inputs represent 3 unit loads each.

Outputs: Each output (0 and 1) is capable of driving 10 unit loads. Two +3V supplies (U1 and V1), capable of 25 unit loads, are available.

Power Dissipation: +5V at 55 mA (average), 100 mA (maximum).

4.5.7 M214 Adder Logic Network

The M214 module contains a 6-bit storage register with input gating logic. Three of these modules are connected in tandem to form the 16-bit Adder network for the RK11 Header and Checksum comparisons and calculations. (Refer to engineering drawing D-BS-RK11-C-15.) Input gating logic is included in the module for strobing the RKDA, RKDB, $\overline{\text{RKDB}}$, and data words into the register.

The following are the input, output, and power characteristics of the M214 module.

Inputs: The following list shows the input connections and TTL unit loading they represent:

Name	Pin	Loading
RKDB → ADD or ADD CRY OUT	U1	4
0 → ADDERS	S1	6
RKDB → ADD	R2	6
RKDA → ADD	R1	6
$\overline{\text{RKDB}}$ → ADD	H1	6
DATA → ADD	M2	6
RKDB	B2, C1, K2, J1, P2, P1	1 each
RKDA	H2, F2, L2, L1, S2, T2 (GND if not used)	1 each
$\overline{\text{RKDB}}$	A1, D2, J2, F1, N2, N1	1 each
CLK ADDERS	V2	6

Outputs: Each ADD output (pins E2, E1, K1, M1, U2, and V1) is capable of driving 9 unit loads and the ADD #1 CRY OUT (pin D1) is capable of driving 5 unit loads. The CLK ADDERS pulse should occur at least 100 ns after the CARRY IN and input data have stabilized. Add outputs should occur 50 ns (maximum) after the module is strobed.

Power: 5V at 280 mA (maximum).

4.5.8 M216 Six Flip-Flops

M216 is a single-height module containing six D flip-flops. All flip-flops operate independently except for their clear line, which is shared among three flip-flops.

Data must be present at the D input 20 ns before the clock pulse and should remain 5 ns after the leading edge of the clock pulse has passed the threshold voltage. The flip-flop settles in 50 ns. The CLOCK, DIRECT SET, and CLEAR inputs must be present for at least 30 ns.

Inputs: Voltages are standard TTL levels.

Pin	Function	Load
B1,D2,H1,L2,N1,S2	C Inputs	2 units
C1,E2,J1,M2,P1,T2	D Inputs	1 unit
D1,F2,K1,N2,R1,U2	DIRECT SET	2 units
A1,K2	DIRECT CLEAR	9 units

Outputs: Voltages are standard TTL levels. Each output is capable of driving 10 unit loads.

Input/Output Delay: 50 ns

Power Dissipation: 435 mW

4.5.9 M238 2 4-Bit Synchronous Counter Module

The M238 is a single-height module consisting of 2 DEC 74193 ICs mounted on the W961 (50-08912). The DEC 74193 is a 4-bit binary, synchronous up/down counter. In the RK11, the M238 application consists of an incrementing function. This incrementing is done by the counter as it represents bits 00 through 07 of the RKDA.

Inputs: All inputs are equivalent to 1 TTL unit load.

Outputs: All outputs can drive 10 TTL unit loads.

Power: Nominal voltage of +5V drawing 204 mA current (pin A2). Pins C2 and T1 are grounded.

4.5.10 M239 Three 4-Bit Counter Register

The M239 is a single-height module that provides independent 4-bit registers that can be parallel loaded, counted, and reset. The M239 is used primarily for counting and data storage. In the RK11, two M239s are used to provide bits 08 through 15 of the RKDA, the INT FUN register, and bits 01 through 04 and 08 through 12 of the RKCS.

Inputs: COUNT/LOAD/RESET are equivalent to 1.25 TTL unit loads each. DATA INPUTS are 1 TTL unit load equivalent.

Outputs: Data Outputs are capable of driving 10 TTL unit loads each.

Power: +5V with a ±5 percent tolerance at 200 mA (A2).

4.5.11 M304 One-Shot Delay – Pulse Amplifier

The M304 module consists of four, one-shot delays internally connected for 1 μs ± 10 percent delay duration. Pins B1, K2, L2, and V1 may be connected to +5V to reduce the delay duration by a factor of 10 approximately. Complementary outputs are provided from each circuit at the pins. Each output is capable of driving 28 unit loads. Each delay may be triggered by a transition from high to low at either of the two inputs of each respective circuit with the other input high. Both inputs must be high for a period greater than 50 ns before triggering at either input. The delay may not be triggered within 50 ns after completion of the timing duration.

For use as a pulse amplifier, pins B1, K2, L2, and V1 may be connected to +5V to cause the delay duration to shorten to approximately 100 ns. The pulse width from either of the complementary outputs should not be less than 70 ns and the trailing edge of the pulse should not be greater than 170 ns from 50 percent of input fall.

For use as a delay the M304 is useful as a 1-μs one-shot delay without connecting B1, etc. Delay accuracy is ±10 percent and is not adjustable. Propagation delay to the leading edge of the low output should be less than 80 ns.

Inputs: Two inputs to each delay function as low OR inputs. One unit load must be provided for each gate. Input signals are differentiated and require that the rate of fall of input signals be greater than 2V/μs.

4.5.12 M307 Integrating One-Shot

The M307 consists of two retriggerable one-shot delays, potentiometers, and capacitors on a single-width double-sided module. Provision is made for selection of one six delay ranging from 0.5 μs to 0.5s by module pin connections. Potentiometers are provided on the module for continuous variation of delay time over a 10-to-1 range.

Inputs:

Low OR inputs: Pins K2 and L2 (U1, S1) constitute a logical low OR input. Delay time commences at the transition of either of these pins from +2V to +0.45V. Loading at each input is 60 μA to +4.2V, 1.6 mA to ground.

When using the inputs K2 and L2 (U1, S1) to trigger the delay, all other inputs must be more positive than 2.4V.

High input: Pin J2 (N1) triggers the delay on the positive transition of the input signal. Loading at this input is the same as above.

When using pin J2 (N1) to trigger the delay, one or both of the low OR inputs must be less than +0.2V and pin L1 (M1) must be more positive than +2.8V.

dc input: A low input to pin L1 (M1) causes the output of the delay to become asserted and remain asserted for a time equal to the time pin L1 (M1) remains at ground plus the time of the delay.

Output: All outputs have a 10 unit load driving capability.

Delay Range:	Pin Connections Circuit 1	Pin Connections Circuit 2
0.5 μs to 5 μs	None	None
5 μs to 50 μs	D1 to D2	U2 to M2
50 μs to 500 μs	B1 to D2	V2 to M2
500 μs to 5 ms	E1 to D2	S2 to M2
5 ms to 50 ms	F1 to D2	R2 to M2
50 ms to 0.5s	H1 to D2	P2 to M2

External capacitors may be connected from pin J1 to D2 (N2 to M1). Electrolytic capacitors must be polarized positive (+) to pin J1 (N2). Wiring to these pins must be extremely short. It is recommended that external capacitors be connected to a W994 blank module and located adjacent to the M307.

Potentiometers are provided on the module for continuous variations of delay time over a 10-to-1 range. To connect the internal potentiometers, connect pin A1 to C1 (V1 to P1). External fine adjustment of the delay time may be accomplished by a Vernier consisting of a 100K rheostat connected from +5V to pin C1 (P1).

Power Requirements:			
	Pin A2	+5V	70 mA
	Pin B2	-15V	0 mA
	Pin C2, T1		GND

4.5.13 M611 Power Inverter Module

The M611 is a single-height module that contains 14 DEC 74H70 high-speed power inverters. The M611 is used in the RK11 for signal inversion to provide high drive compatability of internal signals, for example, the generation of the CLR MSR signal (see Paragraph 3.4.1).

Inputs: Pins A1, D1, F1, E2, J1, H2, L1, K2, N1, R1, P2, V1, S2, and U2 are inputs of the M239 that input 1 TTL fast-series unit load.

Outputs: The output pins of the M239 are B1, E1, H1, K1, J2, M1, L2, P1, S1, R2, U1, T2, and V2. Each output can drive up to 80 TTL unit loads of fast-series gates with D2 as the +3V reference. The worst-case delay is 20 ns, with 30 TTL unit loads. Minimum delay is 10 ns.

4.5.14 M797 Register Selection Module

The M797 is a single-height module used to decode one of eight possible register addresses in conjunction with the M105 module (see Table 4-1 for M105 reference). In addition, control signals are used to select a Read, Write low byte, or Write high byte.

4.5.14.1 Theory of Operation – The M797 contains three BCD/DEC decoders of which outputs 0 through 7 are used to select a register. Outputs 8 and 9 are used to create a gating strobe. The module is enabled by the input at V1 (DEV SELD) at which time the control signals at A1 and D1 select the correct decoder(s) for the operation specified. Once a decoder or decoders has been selected, its 8 and 9 outputs are driven high, asserting STRT XTIM output at H1. One of the 0 through 7 outputs of the decoders is selected by the inputs at B2, B1, and C1. These inputs are inverted before reaching the decoders so that if they are all high the 0 output of the decoder will be selected. The input at V2 can be used to prevent the selection of the two decoders used to write into a register when it is asserted H (i.e., BUSY H). The exception to this is when the three address inputs are high (i.e., selection of a control register). In the RK11, this feature is not used and V2 is grounded.

4.5.15 H734 Power Supply

The H734 Power Supply supplies the dc for the disk drives of the RK11 System. Each H734 supplies power to two drives. The H734 has overvoltage protection with the crowbar at ±16.5 Vdc. The H734 also contains an undervoltage detection of ±13.7 Vdc and low input voltage detection at approximately 100V. Both positive and negative voltages in the H734 are regulated by two switching mode voltage regulators. These two circuits operate from a rectified filtered dc voltage of ±25V ±2V ripple. The regulators contain differential amplifiers that compare the regulator output to a stable reference and adjust the output accordingly to either increase or decrease its level.

Input Voltage:	H734A	115V ± 10% 6A
	H734B	230V ± 10% 3A
Output Voltage:	+15 Vdc ± 5% at 12A	
	-15 Vdc ± 5% at 12A	

CHAPTER 5
INSTALLATION

5.1 INTRODUCTION

RK11 System installation consists of procedures and requirements necessary to achieve operational status. Operational status is achieved through system configuration and installation planning, procedures, and testing.

5.2 SYSTEM CONFIGURATION

The RK11 System configuration depends on the number of disk drives used in a particular system. Figure 5-1 illustrates the equipment housing for up to a maximum of eight disk drives. The only options available on the system are the choices of high or low density drive and the configuring of additional disk drive units. Each RK11 Control can handle a maximum of eight disk drive units. The initial one to four disk drives are housed in the master cabinet with the RK11 Control logic. Also included in the cabinet are the power supplies for the drives and the control, along with the necessary cabling. Additional disk drives are housed in another cabinet with their respective power supplies. Therefore, a second cabinet is necessary when the system is interfacing from five to a maximum of eight disk drive units. (Table 5-1 lists the disk drive options and their definitions and designations.) Cabinets and hardware required to make added disk drives operational are supplied as part of the unit being added. The RK11 cabinets are dedicated cabinets; that is, no peripheral may be installed in any unused space. Failure to observe this requirement may result in lower disk reliability.

5.3 INSTALLATION PLANNING

Installation planning consists of RK11 System requirements or constraints. These requirements are space, power, environmental, and cabling. Compliance with these requirements assures proper and efficient installation of the RK11 Disk Drive Control System.

5.3.1 Power Requirements

Installation power requirements pertain to the power supplies used in the RK11 System and their installation. Discrete or specific power requirements are listed in the specifications section of Chapter 1. Installation power requirements are on a system level.

The RK11 System uses two power supplies: the H720 E (F), and the H734 A (B). A single H720 Power Supply provides +5V and -15V power to the RK11 Control exclusively. The H720 Power Supply is mounted at the bottom front of the master cabinet that houses the RK11 Control. The H734 Power Supply provides power to two of the disk drives mounted in the RK11 Control cabinet. These are drives A and B (see Figure 5-1); the H734 is mounted at the top rear of the RK11 Control master cabinet. The remaining two disk drives in the master cabinet (drives C and D) are powered by a second H734 Power Supply. This power supply is mounted at the bottom rear of the master cabinet. Additional disk drive units (above four) are mounted in another cabinet where they utilize their own power supplies. As in the master cabinet, the first two drives are powered by an H734 Power Supply, mounted as in the master cabinet. These two drives are designated E and F. The remaining possible two disk drives (H and J) are powered by another H734 Power Supply, which is mounted as in the master cabinet. See Chapter 4 for a detailed description of the H734 Power Supply. Refer to *H720 Power Supply Manual* (DEC-11-HR5A-D) for a detailed description of the H720.

Table 5-1
Option Definitions

Option	Definition
RK11-CA	RK11 Control unit for disk drives, interfaces with PDP-11 that uses 115V 50/60 Hz power.
RK11-CB	RK11 Control unit for disk drives, interfaces with PDP-11 that uses 230V 50/60 Hz power.
RK02-XY	RK11 System Diablo Disk Drive that controls the 600K word low-density disk cartridge.
RK04-XY	RK11 System DECpack Disk Drive that controls the 600K word low-density disk cartridge.
RK03-XY	The RK11 System Diablo Disk Drive that controls the 1.2 million word high-density disk cartridge.
RK05-XY	The RK11 System DECpack Disk Drive that controls the 1.2 million word high-density disk cartridge.
	NOTE **The X and Y designations are variable option designations that are substituted for according to the following constraints:** **X = A for 1st drive** **B for 2nd drive** **C for 3rd drive** **D for 4th drive** **E for 5th drive** **F for 6th drive** **H for 7th drive** **J for 8th drive** **Y = A for 115V 50/60 Hz power** **B for 230V 50/60 Hz power**
RK02-XY or RK04-XY	IBM Type 2315 disk cartridge, low-density 12-sector of 614,400 words for DECpack or Diablo low-density disk drives.
RK03-XY or RK05-XY	IBM Type 2315 disk cartridge, high-density 12-sector of 1,228,800 words for DECpack or Diablo high-density disk drives.

The RK11 System can be operated from either 115 Vac or 230 Vac single-phase, 50 or 60 Hz power. Line voltages must be maintained to within ±10 Vac, and the line frequency should not drift more than 01. Hz. A constant frequency should be provided for installation with unstable power supplies.

5.3.2 Space Requirements

Space requirements depend upon the number of cabinets used and the cabinet size. The cabinets are 30 in. by 21-11/16 in. by 71-7/16 in. Both cabinets of the RK11 System must be bolted together in pairs. A dimensional diagram of the RK11 cabinet is shown in Figure 5-2.

Two H911 Mounting Panels are used to house the RK11 Control logic modules. (Refer to Table 4-1 for the list of modules, type, and quantity for the RK11 Control.) These panels have a special end plate for +5V, -15V, GND, AC LO, and DC LO connections to the module connector blocks. The H734 Power Supply is mounted directly above and to the rear of the H911 Mounting Panels. The H911 panels contain rows of module slots labeled A, B, C, and D, from top to bottom, and so referenced in the print set module utilization drawings. Up to four disk drive units can be mounted below the logic. The power supplies are mounted at the bottom of the cabinet with the H720 in the front and the H734 in the rear.

5.3.3 Environmental Requirements

Paragraph 1.3 lists the temperature and humidity requirements for the RK11. All other environmental requirements pertain to the disk drive units used with the RK11. These disk drive environmental requirements are found in the respective manuals for the disk drives supplied in the system.

5.3.4 Cable Requirements

The cable requirements for the RK11 System pertain to the Unibus cable, the disk drive daisy chain cables, and the power wiring. The Unibus cable is 10 ft long and is normally supplied with each RK11. The limiting condition for this cable is the maximum total Unibus cable allowed by the processor. The limit for the PDP-11 is 50 ft. This cable is designated BC11A and plugs into slots A01 and B01 of the logic assembly. Slots A02 and B02 are reserved for a M930 terminator card if the RK11 is the last device on the Unibus or for the Unibus Out cable to the next device. The In and Out slots are not completely parallel wired thus it is impossible to interchange their purposes.

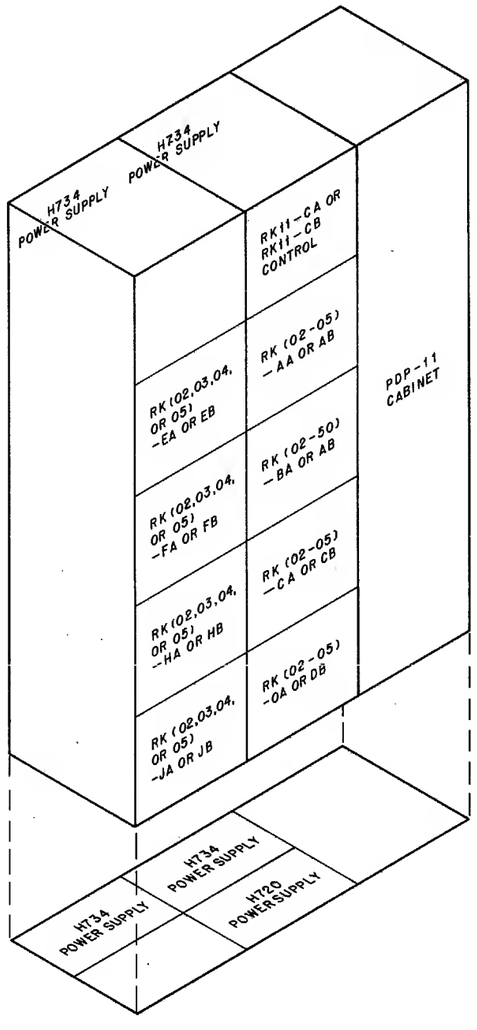


Figure 5-1 RK11 System Configuration

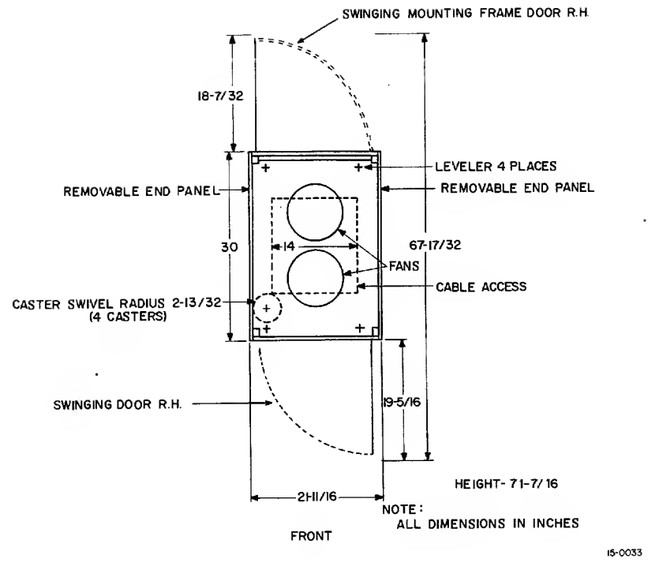


Figure 5-2 The RK11 Cabinet

Drives A through D (four drives of master cabinet) make up a daisy-chain bus of four drives connected directly to the RK11 Control. Drives E through J make up a second daisy-chain bus or four drives that is also connected directly to the RK11 Control. On the inside rear of each disk drive is a jumper plug to determine the physical disk position on a given bus. The first drive on the first daisy-chain bus (bus 1) in logic assembly slots AB12 of the RK11 should be jumpered to position 1 and is designated disk A. The second drive on bus 1 should be jumpered to position 2 and is designated disk B, and so on. Similarly, the first drive on bus 2 (slots AB10 of the RK11 logic assembly) should be jumpered to position 1 and is designated disk E. The second drive on bus 2 should be jumpered to position 2 and is designated disk F, and so on. A detailed discussion of the disk drive cabling is found in the respective manual supplied with the disk drive unit used in the particular system.

The power wiring cabling applies power from the respective power supplies discussed in Chapter 4 to the RK11 and each disk drive. The power wiring cabling for the disk drives is discussed in the respective disk drive manual supplied with the system. Figure 5-3 shows a typical cabling configuration for the RK11 System.

5.4 INSTALLATION PROCEDURE

The RK11 Disk Drive Control System installation procedure consists of unpacking and installing the equipment and power turn-on procedures. The system may arrive at the installation site as either a complete system (with RK11 logic, disk drive unit, power supplies, and the necessary cabinets and mounting panels) or as an add-on (with additional disk drives to be mounted in cabinets already in use at the operation site).

5.4.1 Cabinet Unpacking

If the equipment arrives in cabinets, the following procedure should be followed to unpack and position them.

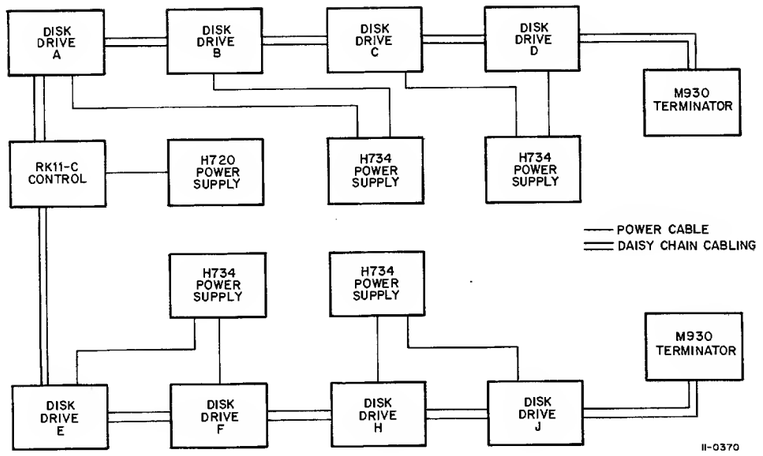


Figure 5-3 Typical Cabling Configuration

Step	Procedure
1	Remove the outer shipping container, which may be either heavy corrugated cardboard or plywood. Remove all straps first and then any fasteners and cleats securing the container to the skid. Remove any wood framing and supports.
2	Remove the Polyethylene covers from all cabinets.
3	Remove the tape or plastic shipping pins from the rear access doors.
4	Unbolt the cabinets from their shipping skids. The bolts can be reached through the rear doors.
5	Raise the leveling feet so that they are above the level of the roll-around casters.
6	Form a ramp with wooden blocks and planks from each cabinet skid to the floor, and roll each cabinet down this ramp.
7	Roll the system to its proper location.

5.4.2 Cabinet Installation

The disk drive cabinets are equipped with roll-around casters and adjustable leveling feet. They have to be leveled. In multiple cabinet installations, cabinets are shipped in pairs. The cabinets should be connected together at the site. To install the cabinets, the following procedure should be used:

Step	Procedure
1	Cabinets are joined by filler strips (see Figure 5-4). After the cabinets are positioned, put the cabinets together and bolt both filler strips and cabinets together. Do *not* tighten the bolts securely.
2	Lower the leveling feet until they support the cabinet. Using a spirit level, check that all cabinets are level and that the feet are firmly against the floor.
3	Tighten the bolts that hold the cabinets together and again check the leveling.
4	Remove the shipping bolts and tape from the slide runners of each disk drive.
5	Run a ground strap from the DECdisk cabinets to the PDP-11 cabinet.

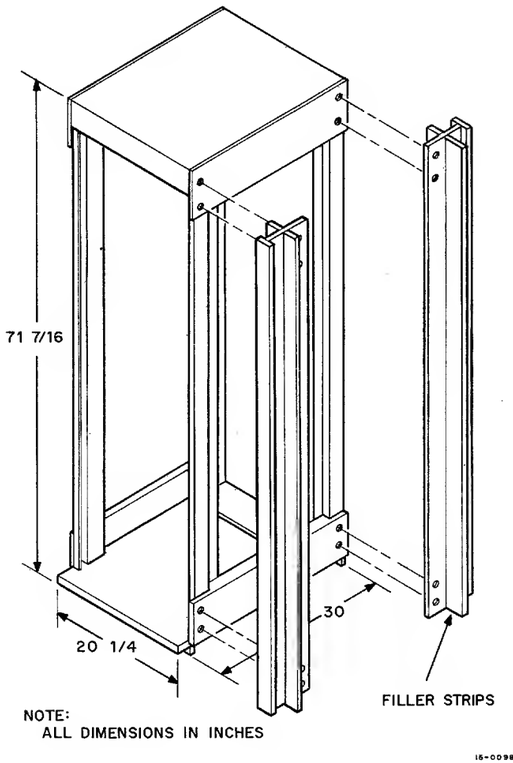


Figure 5-4 Cabinet Bolting Diagram

5.4.3 RK11 Installation

The RK11 Control comes mounted in a cabinet (master cabinet) with at least one disk drive unit. To install the RK11 Control unit:

Step	Procedure
1	Check that the wiring is not damaged, that hold down bars are in place, and that no modules have fallen out.
2	Install the Unibus cable according to the *PDP-11 Unibus Interface Manual* (DEC-11-HIAA-D) and install the Disk Drive cabling; drives 0–3 AB12 and drives 4–7 AB10.
3	Connect all the power wiring for the system.

5.4.4 Disk Drive Unpacking and Installation

The information for unpacking and installing the disk drive supplied with the particular RK11 System is described in the respective manual for the disk drive and supplied with the disk drive.

5.4.5 Power Turn-On Procedure

The following steps are required to power up the RK11 to operational status:

Step	Procedure
1	Turn cabinet power on.
2	Disk drive doors will unlock.
3	Open disk drive door.
4	Insert the proper disk cartridge.
5	Move the RUN/LOAD switch to RUN.
6	In approximately 50s, the READY light will illuminate on the disk drive front panel. The disk is now ready for on-line operation.

5.5 INSTALLATION TESTING

Installation testing is performed to ensure that the RK11 System is properly installed and operational. This is achieved through the running of two of the RK11 diagnostic programs. First, one pass of the RK11-C disk data test (MainDEC-11-D5HA-PB2) is run and then 15 minutes of the RK11-C static test (MainDEC-11-D5HA-PB1). If no errors are detected from the performance of these tests, the RK11 is operational and has been installed correctly. These diagnostics are supplied with the RK11, along with instructions and descriptions of the diagnostics. Refer to Paragraph 6.3 for a discussion of the diagnostic programs.

CHAPTER 6
MAINTENANCE

6.1 INTRODUCTION

RK11 maintenance is accomplished through the performance of an inspection procedure, a diagnostic software procedure, and the operation of the hardware maintenance modules. The inspection procedure is a preventive maintenance check of the RK11's System components for visual defects. The diagnostic software procedure consists of running the three MainDEC programs to isolate an RK11 hardware malfunction. These diagnostics are primarily trouble-shooting tools and check total system operation with the disk drives on-line. The RK11 maintenance modules are also trouble-shooting tools that reflect specific hardware states through their indicator-light network using the exclusive RK11 Indicator overlays.

6.2 INSPECTION PROCEDURE

The inspection procedure provides a visual check of the RK11 System by performing the steps listed in Table 6-1.

6.3 DIAGNOSTICS

The RK11-C software trouble-shooting system diagnostics consist of three MainDEC programs: MainDEC-11-D5HA-PB1 (static test), MainDEC-11-D5HA-PB2 (disk data test), and MainDEC-11-D5GA (random seek exerciser). These programs, along with program listings, are supplied with each RK11-C shipped. The program listings contain program descriptions and explanations, along with instructions for running the diagnostics. Running the diagnostic programs provides a hardware trouble-shooting feature for locating hardware malfunctions.

6.4 MAINTENANCE MODULES

The maintenance modules consist of two W130 Maintenance Connector Modules and two W131 Maintenance Indicator Modules. These modules are PDP-11 available options for general hardware maintenance functions. (Refer to engineering drawings D-CS-W130-0-1 and D-CS-W131-0-1 for the W130 and W131 circuit schematics, respectively.) The W131 connects specified RK11 internal logic states to the W131 for indicator display. The W131 consists of an indicator-light network that is fitted with overlays (one for each W131) that reflect the RK11 logic state to which the W130 is connected. Figure 6-1 shows the two RK11 overlays for the W131's, along with the RK11 logic states that the indicator on-state will reflect. The RK11 also utilizes one of the switches on each of the W131's. The following procedure lists the general features for using the maintenance modules with the RK11-C overlays.

Table 6-1
Visual Inspection Checklist

Item	Check
Mechanical Connections	*a.* Check that all screws are tight and that all mechanical assemblies are secure. *b.* Check that all crimped lugs are secure and that all lugs are properly inserted in their mating connectors.
Wiring and Cables	*a.* Check all wiring and cables for breaks, cuts, frayed leads, or missing lugs. Check wire wraps for broken or missing pins. *b.* Check that no wire or cables are strained in their normal positions or have severe kinks. Check that cables do not interfere with doors, and that they do not chafe when doors are opened and closed.
Modules and Components	Check that all modules are properly seated. Look for areas of discoloration on all exposed surfaces. Check all exposed capacitors for signs of discoloration, leakage, or corrosion. Check power supply capacitors for bulges.
Indicators and Switches	Check all indicators and switches for tightness. Check for cracks, discoloration, or other visual defects.

Step	Procedure
1	In the lower left-hand corner of the RK11-C logic assembly are two female 36-pin module slots. These slots are connected to flexible cables with M922 Module connectors at the end. These connectors are normally plugged into slots A30 and B30 of the RK11 logic assembly.
2	Plug the W130 Module into the female connector located on the lower left-hand corner of the RK11-C logic assembly.
3	Plug the W131 into the W130 for each pair.

(continued on next page)

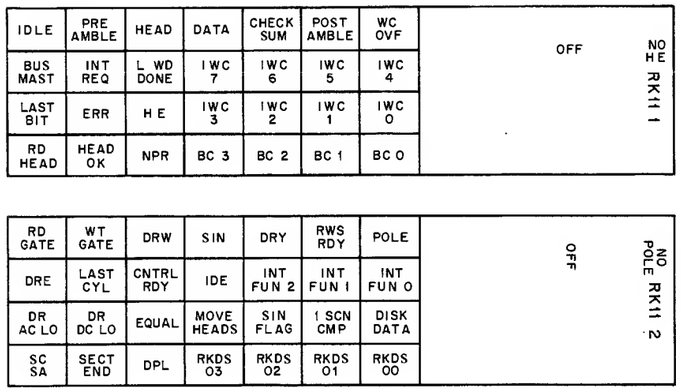


Figure 6-1 W130 and W131 Maintenance Indicator Overlays

Step	Procedure
4	The RK11-C maintenance overlays fit over the plastic front cover of the W131 to identify the various W131 lights and switches. Overlay no. 1 should connect to slot A30 and overlay no. 2 should connect to slot B30. This provides the user with 28 lights per overlay to visually monitor the internal operations of the RK11-C Control. With two sets of maintenance modules the user can monitor a total of 56 logic states or lights simultaneously.
5	Overlay no. 1 has a switch marked NO HE. When the switch is in this position, the Hard Error (HE) flip-flop in the RK11 Control cannot set.
6	Overlay no. 2 has a switch marked NO POLL. When the switch is in this position the hardware poll function cannot function.